IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

In re: REMBRANDT TECHNOLOGIES, LP PATENT LITIGATION	**MDL Docket No. 07-md-1848 (GMS)**

REMBRANDT'S OPENING CLAIM CONSTRUCTION BRIEF RE '627 PATENT

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I. OVERVIEW OF THE '627 PATENT

The '627 patent (U.S. Patent No. 5,243,627, at A001-A012, also attached as Ex. 1) generally relates to error correction in digital transmission systems. In such systems, a sequence of digital data is transmitted by a transmitter across a transmission channel to a receiver, typically by modulating an analog waveform using the digital data. Modulation entails altering characteristics (i.e., phase, frequency, amplitude or a combination thereof) of this analog waveform to represent the digital data. The analog waveform is received by the receiver and demodulated to recover the transmitted digital data. (Ex. 1 at 5:48-56).

A basic problem in the design of such data transmission systems is how to eliminate the effect of "noise" introduced into the data signal during transmission. This noise, which may result for example from environmental factors or imperfections in the transmission or reception equipment, can modify the characteristics of the modulated analog waveform so that the signal received is different from what was transmitted. Such noise can "worsen the effectiveness of the . . . receiver to recover the transmitted data." (Ex. 1 at 1:31-33).

To mitigate the problems caused by noise, digital transmission systems typically include some type of error correction coding to aid in the recovery of the transmitted signal. (U.S. Patent No. 4,677,625, at B001-B008, also attached as Ex. 2 ("the '625 patent") at 1:23-37). One type of error-correction coding uses a "trellis encoder" to encode data in the transmitter and a "Viterbi decoder" to decode data in the receiver. (Ex. 2 at 2:44-45, 3:21-29).[1]

The trellis encoder adds "redundant bits . . . systematically to the data bits" to be sent before modulation. (Ex. 2 at 1:37-41). There is an "inherent correlation between these

[1] The name "trellis" encoder derives from state diagrams used to map out the most likely data sequences, which look like an ivy-covered trellis typically set against a country home. Viterbi decoders get their name from the Viterbi algorithm used to detect and correct errors in transmitted data.

redundant bits," which is used to help the receiver recover transmitted data that is lost because of noise. (Ex. 2 at 1:41-43). It is this correlation that sets up predetermined sequences of bit transitions (resembling a trellis lattice, *see* App. at B009 illustrating an exemplary trellis diagram) representing all of the possible sequences of bits that could have been transmitted. Because "only predetermined transitions from one sequential group of bits . . . to another" are allowed, the Viterbi decoder is able to determine from a received sequence of bits whether that sequence is erroneous—i.e., whether it fails to follow the prescribed pattern of transitions—and if so, to estimate the most likely sequence that was actually transmitted. (Ex. 2 at 1:37-41).

Viterbi decoders, however, can fail to properly correct errors when "relatively long error signals" occur, i.e., bursts of noise that affect a sequence of transmitted data over an extended period of time (also referred to as "burst errors" as distinguished from "random errors" which affect intermittent portions of transmitted data). (Ex. 2 at 1:46-50). When burst errors occur, a Viterbi decoder loses its ability to correct data streams because too many errors occur among the correlation of bits generated by the trellis encoder. The '627 patent refers to such error signals as "correlated noise" which "inhibits the correction of received bits" using Viterbi decoders because too many successive received data values are erroneous. (Ex. 1 at 7:5; Ex. 2 at 1:46-51). The closest valid sequence as determined by the Viterbi decoder may not be the sequence that was actually transmitted. Burst errors are pervasive and occur frequently in digital transmission and present a real problem in practical applications.

The '627 patent, issued to William Betts and Edward Zuranski, teaches a novel mechanism, called "signal point interleaving," for reducing the vulnerability of Viterbi decoders to burst errors (i.e., correlated noise). As the '627 patent explains, this mechanism represents an

improvement over an earlier technique called "channel symbol interleaving" that was disclosed by Mr. Betts and others in the prior art '625 patent. (Ex. 1 at 1:33-2:2).

The earlier channel symbol interleaving technique entailed using multiple trellis encoders in a single transmitter, and multiple corresponding Viterbi decoders in the corresponding receiver, to improve the correction of errors caused by correlated noise. (Ex. 2 at 2:27-29, 3:13-18; Ex. 1 at 1:34-38). In the preferred embodiment of the '625 patent, the transmitter comprised a "distributed trellis encoder" having four distinct trellis elements, as shown in Figure 1 of the '625 patent. To accomplish channel symbol interleaving, data was sent to the individual trellis encoders in "round-robin fashion," meaning the trellis encoders would take turns operating on data. (Ex. 1 at 1:59-62). Accordingly, only the currently "active" trellis encoder would encode data, while the "other . . . trellis encoders are idle." (Ex. 2 at 2:50-52). The receiver in the '625 patent would use a corresponding distributed Viterbi decoder to decode the received data (Ex. 1 at 1:62-65; Ex. 2 at 2:2-4, 3:67-4:3). Like the distributed trellis encoders, the distributed Viterbi decoders operated in a round-robin fashion, so that only one Viterbi decoder was active at a time. (Ex. 2 at 3:43-49). As a result, each Viterbi decoder in the receiver only decoded that data which was generated by a corresponding trellis encoder in the transmitter. (Ex. 2 at 3:47-55).

The advantage of using multiple, corresponding pairs of round-robin activated trellis encoders and Viterbi decoders, as opposed to a single conventional trellis encoder/Viterbi decoder pair, lay in the resulting "interleaving" of data transmitted between the respective pairs of encoders and decoders. (Ex. 1 at 1:59-2:2). In particular, the round-robin mechanism caused "channel symbols" from a given trellis encoder—values representing successive chunks of data processed by the trellis encoder—to be separated from each other on the transmission channel. (Ex. 1 at 1:59-2:2). The Figure at B010 illustrates the resulting pattern of channel symbols on

the transmission channel, with each color representing channel symbols that are encoded and decoded by respective trellis encoder/decoder pairs. (Ex. 1 at 1:59-2:2).

As can be seen from this pattern, no two channel symbols associated with a given trellis encoder/decoder pair are adjacent to each other on the transmission channel. (Ex. 1 at 1:59-2:2). As a result, correlated noise would have to last longer to affect enough channel symbols from any given trellis encoder to prevent their accurate reception by the corresponding Viterbi decoder. (Ex. 1 at 1:49-52). For example, consider a burst of noise that impairs the values of four consecutive channel symbols in the stream above. If all the channel symbols were to be processed by a single encoder/decoder pair, the Viterbi decoder would have to correct four successive erroneous values, possibly overwhelming its ability to recover the original data stream. (Ex. 2 at 1:41-52). However, when the noise impacts channel symbols from four separate trellis encoder/Viterbi decoder pairs operating in a round-robin fashion, each Viterbi decoder would only need to decode one of the four erroneous channel symbols, thereby reducing the likelihood that any given Viterbi decoder would fail to make the proper error correction. (Ex. 2 at 3:61-64).

The improvement of the '627 patent comprises augmenting the channel symbol interleaving technique disclosed in the '625 patent with an additional technique called "signal point interleaving." (Ex. 1 at 2:11-24). Whereas the channel symbol interleaving of the '625 patent provides a way of reducing the amount of correlated noise seen in successive channel symbols transmitted between a given trellis encoder/Viterbi decoder pair, the addition of signal point interleaving takes this concept a step further by reducing the amount of correlated noise within a single channel symbol. (Ex. 1 at 1:59-2:2).

As in the '625 patent, the transmitter of the '627 patent features a "distributed trellis encoder" comprising, in the preferred embodiment, "three trellis encoder stages" that operate in a round-robin fashion as illustrated in Figure 3 (reproduced with highlighting at B011). (Ex. 1 at 4:64-5:5). Three trellis encoder stages, 319α, 319β, and 319γ, perform channel symbol interleaving in a manner essentially the same as that taught in the '625 patent (Ex. 1 at 4:64-5:13): successive channel symbols generated using a given trellis encoder stage are separated from one another by other channel symbols generated using the other two trellis encoder stages. As in the '625 patent, this reduces the likelihood of correlated noise affecting successive channel symbols to be decoded by the same Viterbi decoder stage.

What the inventors of the '627 patent discovered was that the data within the channel symbols of the '625 patent remained vulnerable to correlated noise, which Viterbi decoders could not correct. (Ex. 1 at 2:5-13, 6:67-7:6). Reducing correlated noise within a single channel symbol is advantageous in coding systems where larger amounts of data are allocated to each trellis encoder every time a trellis encoder is active. (Ex. 1 at 6:67-7:6, 8:3-9). Larger inputs fed into each active trellis encoder produce larger trellis encoded channel symbol outputs. (Ex. 1 at 3:52-4:3). These larger channel symbol outputs often need to be sent in more than one signaling interval.

To solve this problem, the inventors of the '627 patent recognized that the generated channel symbols could be formed of more than one signal point and, therefore, be divisible. The divisibility of the channel symbols into constituent signal points is what allows the data within channel symbols to be interleaved. (Ex. 1 at 2:5-13).

For example, the trellis encoded channel symbol shown in Appendix at B012 is too large to be modulated by the transmitter in one "signaling interval"—a unit of time corresponding to

how much digital data can be represented at once on an analog waveform to be transmitted to the receiver. (Ex. 1 at 2:21-28, 3:38-42). Instead, it is composed of multiple "signal points," each of which can be modulated during a single signaling interval. (Ex. 1 at 3:38-42, 3:52-4:3). As shown at B012, therefore, it takes two signaling intervals to modulate and transmit the trellis encoded channel symbol from the transmitter to the receiver, with one signal point being modulated and transmitted during each signaling interval. (Ex. 1 at 3:38-42).

The effect of this optimization on the transmission pattern of signal points can be seen in two sequences found at B013, which are taken from Figure 5 of the '627 patent (with color highlighting added). Both sequences show the signal points that make up the channel symbols generated using respective trellis encoder stages 319α, 319β, and 319γ. In the first sequence, where only the invention of the '625 patent is used, the channel symbols are not divided. As a result, while the channel symbols generated by the different trellis encoders are spaced apart from each other (e.g., channel symbol $[X_0^{\alpha} X_1^{\alpha}]$ is spaced apart from channel $[X_6^{\alpha} X_7^{\alpha}]$), the component signal points of each channel symbol remain adjacent to each other. (Ex. 1 at 7:1-6). "[S]ince all the signal points of a channel symbol must be processed serially by the same Viterbi decoder stage, this means that the Viterbi decoder must process adjacent signal points that have highly correlated noise components." (Ex. 1 at 7:1-6).

By contrast, in the second sequence, which was generated using the invention of the '627 patent, there is a separation of at least three signaling intervals between: (a) the signal points which belong to any particular channel symbol, and (b) the signal points which belong to successive channel symbols output by a given trellis encoder. (Ex. 1 at 7:55-64). This combination of signal point interleaving and channel symbol interleaving reduces the effect of

correlated noise during transmission and improves the ability of the Viterbi decoder stages to correctly decode the transmitted signal. (Ex. 1 at 7:55-8:2).

II. PRIOR CONSTRUCTION OF THE '627 PATENT

The claim terms of the patents-in-suit were previously construed in *Rembrandt Technologies, L.P. v. Comcast Corp.*, Civ. No. 2:05-CV-443 (TJW) (E.D. Texas) ("Texas Court").[2] Although the Texas Court's Order construing the claims is not binding in this action, it addresses many similar issues of claim construction as presented here and can be viewed as "persuasive and highly relevant . . . authority." *Verizon Cal. Inc. v. Ronald A. Katz Tech. Licensing, L.P.*, 326 F. Supp. 2d 1060, 1069 (C.D. Cal. 2003).

In *Markman v. Westview Instruments, Inc.*, 517 U.S. 370 (1996), the United States Supreme Court noted that *stare decisis* favors promoting uniformity in claim construction. Even though a court's previous claim construction order does not necessarily collaterally estop a new defendant on issues of claim construction, courts have frequently deferred to a previous claim construction determination if new evidence has not been presented by the defendant. *See KX Indus., L.P. v. PUR Water Purification Prods., Inc.*, 108 F. Supp. 2d 380, 387 (D. Del. 2000).

Furthermore, adopting a prior claim construction order is generally in the interest of maintaining consistency between copending actions, and promotes judicial efficiency. *See, e.g., Zoltar Satellite Sys. v. LG Elecs. Mobile Commc'ns Co*, 402 F. Supp. 2d 731, 737 (E.D. Tex. 2005) ("[I]nconsistent claim constructions of the same claims by different courts can create serious problems. . . . These problems especially deserve consideration when the same patent is simultaneously being litigated in another district."). *See also Atmel Corp. v. Silicon Storage*

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[2] Copy of the relevant claim construction order from *Rembrandt Technologies, L.P. v. Comcast Corp.* is at B019-B040. Also at B014-B016 is a comparison claim chart including Texas Court's, Rembrandt's, and All Other Parties' proposed constructions.

Tech., Inc., 2001 U.S. Dist. LEXIS 25641 (N.D. Cal. June 20, 2001) (Court adopted previous claim construction from plaintiff's lawsuit against another party).

III. EXEMPLARY CLAIM OF THE '627 PATENT

Independent claim 19 provides an example of the claims at issue in this case. The claim begins by requiring:

> *A method for use in a receiver to recover information from a received stream of trellis encoded signal points,*

The claim then shifts focus to the transmission side, describing how the received stream of signal points is created in the transmitter:

> *said signal points having been transmitted to said receiver apparatus by a method which includes the steps of*

Consistent with the patent's teaching of multiple trellis encoders, the claim indicates that these signal points must be generated as part of two or more "streams" of trellis encoded channel symbols:

> *generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said information,*

Each of these trellis encoded channel symbols have multiple signal points:

> *each of said channel symbols being comprised of a plurality of signal points,*

To form a stream of these signal points for transmission, there is an interleaving process that takes place:

> *interleaving the signal points of said generated channel symbols to form said stream of trellis encoded signal points,*

As discussed above, the required interleaving separates the data in two ways: the interleaving must separate the signal points within a given channel symbol, i.e., they must be "non-adjacent":

said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points

The interleaving must also separate the channel symbols emanating from each trellis encoder stage:

and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points,

The focus then returns to the receiver side:

said method comprising the steps of

On the receiver side, the interleaving process that took place in the transmitter is reversed:

deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols, and

The claimed method also includes using a Viterbi decoder with multiple stages to recover the information transmitted using the signal points:

using a distributed Viterbi decoder to recover said information from the deinterleaved signal points.

IV. THE DISPUTED TERMS

A. "signal point" (claims 1, 2, 9, 10, 11, 12, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a value that is transmitted by a modulator in one signaling interval.*

Rembrandt's proposed construction of "signal point" was adopted by the Texas Court and is consistent with its usage in the claims and the patent specification. The '627 patent teaches that a transmitter uses a modulator to transmit signal points to the receiver. "The signal point . . . is passed on to the modulator 128 to generate a pass-band line signal which is applied to the communication channel." (Ex. 1 at 3:38-42). Each signal point on the communication channel corresponds to a value transmitted in one signaling interval. The signal point generated in the "*n*th baud [or signaling] interval" is passed to the modulator for transmission. (Ex. 1 at 3:38-42).

This is also shown by reference to the number of signal intervals that separate signal points on the communication channel during transmission. As one of many examples, the patent specification describes signal point X_1^{α} in the stream of signal points X_1^{α}, X_2^{α}, X_3^{α}, X_4^{α}, X_5^{α}, X_6^{α} as being separated from the signal point X_6^{α} by five signaling intervals, clearly demonstrating that a signal point gets transmitted every signaling interval. (Ex. 1 at 6:58-61).

All Other Parties, however, assert that the term "signal point" should be construed to require "a point on a 2-dimensional constellation having a pair of coordinates representing two components of a corresponding signal." Evidently, they seek to limit "signal point" to the preferred embodiment, i.e., a value in a two-dimensional modulation scheme such as quadrature amplitude modulation ("QAM"). Neither the specification nor the claims require such a limitation on dimensionality. On the contrary, the patent specification states that: "the invention can be used with signaling schemes of any dimensionality." (Ex. 1 at 8:59-61). *See PHT Corp. v. Invivodata, Inc.*, Civ. No. 04-60-GMS, 2005 U.S. Dist. LEXIS 9577, *23 (D. Del. May 19, 2005) ("where a specification does not require a limitation, that limitation should not be read from the specification into the claims" (quoting *Intel Corp. v. U.S. Int'l Trade Comm'n,* 946 F.2d 821, 836 (Fed. Cir. 1991) (citation omitted))); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect.").

Moreover, All Other Parties' construction violates the doctrine of claim differentiation – because every patent claim is presumptively different in scope, expressly limiting the dimensionality of "signal point" in certain claims compels a broader construction of "signal point" in other claims. *See Comark Communs. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998). Claims 3-5, 8, 13-15, 18 and 23-24 further limit "signal point" to 2-dimensional signal

points. For instance, dependent claim 13 recites "[t]he method of claim 11 wherein said channel symbols are 2N-dimensional channel symbols . . . ." Thus, the claim further limits "signal point" to a 2-dimensional signal point. (Ex. 1 at 4:9-11) ("The concatenation of the N *two-dimensional signal points* thus selected is the desired 2N-dimensional channel symbol." (emphasis added)). Accordingly, it would be improper to limit the construction of "signal point" to any dimensionality. All Other Parties' construction should thus be rejected.

B. "distributed Viterbi decoder" (claims 9, 10, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a Viterbi decoder having multiple Viterbi decoding processes operating on separate portions of a stream of data to be decoded.*

Rembrandt's proposed construction of "distributed Viterbi decoder" was adopted by the Texas Court and gives the term its full scope supported by the patent specification. For example, in one embodiment, the distributed Viterbi decoder is depicted in Figure 4 of the '627 patent as consisting of multiple separate Viterbi decoder stages which receive and process separate portions of a data stream generated on the transmitter side: "signal points . . . are . . . distributed . . . to a distributed Viterbi decoder comprised of 4D Viterbi decoder stages 419α, 419β and 419γ." (Ex. 1 at 6:12-26). The patent specification makes clear, however, that the distributed Viterbi decoder could also be implemented in software as a decoder with a single stage that continually switches the input data to the decoder stage, making it function effectively as a decoder with multiple stages. Thus, a single software program that emulates the function of multiple physical devices can be employed: "[M]ultiple . . . decoders can be realized using a single program routine which, through the mechanism of indirect addressing of multiple arrays within memory, serves to provide the function of each of the multiple devices." (Ex. 1 at 9:61-66).

C. "distributed Viterbi decoder for recovering (to recover) said information from the deinterleaved signal points" (claims 9, 10, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a Viterbi decoder having multiple Viterbi decoding processes operating on separate portions of a stream of deinterleaved signal points to recover the information encoded therein.*

In the context of the claim language, and as fully supported by the patent specification, the distributed Viterbi decoder recovers the transmitted data information. All Other Parties, however, urge the court to construe the distributed Viterbi decoder in a manner that limits its scope beyond the wording used in the claim. Specifically, they urge the court to improperly import a requirement that "*all* of the deinterleaved signal points of a trellis encoded channel symbol" must be received before they are processed by the distributed Viterbi decoder. There is nothing in the claims or specification that supports an inference that the decoder cannot operate on the signal points as they are received. *See PHT Corp.*, 2005 U.S. Dist. LEXIS 9577, at *23 ("[J]ust as the preferred embodiment itself does not limit claim terms, . . . mere inferences drawn from the description of an embodiment of the invention cannot serve to limit claim terms." (quoting *Johnson Worldwide Assoc. v. Zebco Corp.*, 175 F.3d 985, 992 (Fed. Cir. 1999))).

D. "trellis encoded channel symbol" (claims 1, 2, 9, 10, 11, 12, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a set of one or more trellis encoded signal points that corresponds to a group of bits that is treated as a unit by an encoding system.*

Rembrandt's proposed construction of the term "trellis encoded channel symbol" was adopted by the Texas Court and is fully consistent with and supported by the intrinsic record. The patent specification specifically describes how to identify a trellis encoded channel symbol:

> *Serial-to-parallel converter 115 . . . provides, during each succession of symbol intervals, . . . some predetermined number of parallel bits on lead 109* and some number of parallel bits on lead 108 . . . [T]he words on lead 109 are used by trellis encoder 119α to sequentially identify on lead 121N [sic "121 N"] subsets, while the words on lead 108 are used to generate N corresponding index values on lead

117. *The N signal points identified in this way are the component signal points of a 2N-dimensional [trellis encoded] channel symbol.*

(Ex. 1 at 2:61-3:58) (emphasis added). Thus, according to the '627 patent, a channel symbol is the output of the trellis encoding process corresponding to a group of input bits ("on lead 109") that are presented to the trellis encoding mechanism. This group of bits is used to form, and thus correspond to, the trellis encoded channel symbol generated by the trellis encoding mechanism. Therefore, Rembrandt's proposed construction should be adopted.

E. "trellis encoded channel symbol ... comprised of a plurality of signal points" (claims 1, 2, 9, 10, 11, 12, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a set of two or more trellis encoded signal points that corresponds to a group of bits that is treated as a unit by an encoding system.*

As described in the previous subsection, a trellis encoded channel symbol is a set of one or more signal points. The addition of a "plurality" limitation merely requires that the channel symbol comprise two or more signal points. A review of the '627 patent specification shows that these channel symbols are comprised of multiple signal points. (Ex. 1 at 4:9-11). All Other Parties' construction, however, seeks to inject into the claim the additional requirement that the signal points are to be "selected using the same group of parallel input bits as expanded once by a trellis encoder." Claim construction starts and ends with the wording of the claim. Because All Other Parties' proposed construction adds unstated limitations into the claim, it is incorrect. *See Northern Telecom Ltd. v. Samsung Elecs. Co.*, 215 F.3d 1281, 1290 (Fed. Cir. 2000) ("This court has repeatedly and clearly held that it will not read unstated limitations into claim language."). Therefore, All Other Parties' proposed construction should be rejected.

F. "stream[] of trellis encoded channel symbols" (claims 1, 2, 9, 10, 11, 12, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *a sequence of trellis encoded channel symbols.*

The phrase "trellis encoded channel symbol" should be construed as discussed in Section (IV)(D), *supra*. Furthermore, All Other Parties agree that the term "stream" means "sequence." Thus, Rembrandt's proposed construction is complete and correct.

All Other Parties' proposed construction adds the limitation that "each symbol's signal points are adjacent." This requirement is found nowhere in the claims and drawing it out of the specification is improper and should therefore be rejected. *See Northern Telecom*, 215 F.3d at 1290; *SRI International v. Matsushita Electric Corp.*, 775 F.2d 1107, 1121 n.14 (Fed. Cir. 1985) ("Specifications teach. Claims claim.").

Furthermore, All Other Parties' construction would also require that the channel symbols be generated with adjacent signal points *before* the signal points are interleaved. Nowhere in the intrinsic record, however, is there any temporal or sequential constraint that generation of adjacent signal points of a channel symbol occurs *before* interleaving them. The effect of All Other Parties' construction is to bootstrap a temporal restraint onto the order of channel symbol generation and signal point interleaving. *See Baldwin Graphic Sys. v. Siebert, Inc.*, 512 F.3d 1338, 1346 (Fed. Cir. 2008) (holding disclosure of "[a] cleaning fabric with a reduced air content is wrapped around the core to form a fabric roll" did not require "that air content reduction must occur prior to winding"). Therefore, All Other Parties' construction should be rejected.

G. "interleaving the signal points of said generated channel symbols to form said (a) stream of trellis encoded signal points" (claims 1, 2, 9, 10, 11, 12, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *to interleave signal points of trellis encoded channel symbols to form a stream of trellis encoded signal points.*

Rembrandt's construction is fully consistent with and supported by the intrinsic record. The '627 patent explains that, in the exemplary embodiment depicted in Figure 3:

> the stream of signal points X_0^{α}, X_1^{α}, X_2^{β}, X_3^{β}, X_4^{γ}, X_5^{γ}, X_6^{α} . . . which is comprised of three *interleaved streams of trellis encoded channel symbols* . . . [is]

> supplied, in accordance with the invention, to *signal point interleaver 341* which applies alternate ones of the signal points applied thereto to lead 3412 . . . and to one-symbol (Z^{-1}) delay element 3411, which appear on lead 342 after being delayed therein by one symbol interval. The resulting interleaved stream of trellis encoded signal points is X_0^{α}, X_{-1}^{γ}, X_2^{β}, X_1^{α}, X_4^{γ}, X_3^{β}, X_6^{α}, X_5^{γ}, X_8^{β}, X_7^{α}, X_{10}^{γ}, X_9^{β} . . . .

(emphasis added) (Ex. 1 at 5:25 – 39; Fig. 5, ln. V). Thus, the resulting stream of trellis encoded signal points is interleaved in such a way that "the signal points of each channel symbol are non-adjacent" and "the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent," as dictated by the claims themselves. (Ex. 1 at Claims 1, 9, 11, 19 and 21).

All Other Parties' proposed construction, "separating the adjacent signal points of each generated trellis encoded channel symbol using other signal points," fails to consider the claim in its entirety. *See Searfoss v. Pioneer Consol. Corp.*, 374 F.3d 1142, 1149 (Fed. Cir. 2004) (claim construction begins and ends with the actual wording of the claim). Their construction ignores that "said interleaving [be] carried out in such a way that . . . the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent . . . ." (Ex. 1 at Claims 1, 9, 11, 19 and 21). All Other Parties' construction, instead, only addresses interleaving "signal points of each generated trellis encoded channel symbol . . . ." Furthermore, were this Court to adopt All Other Parties' construction, it would also effectively read the preferred embodiment out of the claim. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (A claim interpretation that reads out of a preferred embodiment "is rarely, if ever, correct and would require highly persuasive evidentiary support . . . .").

Moreover, as discussed above, the claim language does not require that the signal points be adjacent, and certainly does not require that the signal points be adjacent *before* they are interleaved. *See* section (V)(F), *supra*. Thus, All Other Parties' construction should be rejected.

H. "deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols" (claims 9, 10, 19, 20, 21, and 22)

Rembrandt's Proposed Construction: *to reverse the process of interleaving performed in the transmitter to recover multiple streams of trellis encoded channel symbols from the interleaved signal points.*

As previously discussed, the interleaving function requires that both, "the signal points of each channel symbol are non-adjacent" and "the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent . . . ." The process of deinterleaving as explained in the '627 patent is merely a reversal of this interleaving function. Through the preferred embodiment, as depicted in Figures 3 and 4, the patent sets forth that the "received signal points are deinterleaved in signal point deinterleaver 441, which provides the *opposite function* to interleaver 341 in the transmitter." (emphasis added) (Ex. 1 at 5:67-6:2). In order to complete the reversal, the channel symbols must be deinterleaved by switching circuit 431 so that they can be fed into the multiple decoder stages: "The received signal points on lead 442 are . . . distributed by switching circuit 431 . . . to a distributed Viterbi decoder . . . ." (Ex. 1 at 6:12-20).

However, as discussed above with respect to the construction of the term "interleaving," All Other Parties' construction continues to effectively read the preferred embodiment out of the claim by disregarding the channel symbol deinterleaving performed by the switching circuit 431. Accordingly, it should be rejected.

I. "Receiver apparatus" (claims 9, 10, 19, and 20)

Rembrandt's Proposed Construction: *a device that receives a transmission signal.*

Rembrandt's construction of the term "receiver apparatus" gives the term its full scope consistent with its ordinary and customary meaning and is fully supported by the patent specification. The patent specification refers to the term as a simple receiver. (Ex. 1 at 1:62-65). At the time of the invention, a person of ordinary skill in the art would understand the term

"receiver" to mean "any device which receives a transmission signal." (Newton's Telecom Dictionary, 4th edition, 1991, at B017-B018).

The "receiver apparatus" cannot, however, be properly interpreted to mean "a device that *demodulates* a received signal and recovers information in the form of a *serial bit stream*," which is contrary to the customary and ordinary meaning of the term. Yet again, All Other Parties seek to import limitations by limiting a receiver to a demodulator that must recover a serial bit stream. Accordingly, their proposed construction should be rejected.

J. "means for generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said input information" (claims 1, 2, 21, and 22)

Rembrandt's Proposed Construction: *interpreted under 35 U.S.C. § 112, ¶ 6.*

Function: generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said input information.

Structure: *a distributed trellis encoder that implements multiple trellis encoding processes operating on respective portions of input information.*

The parties agree upon function. With regard to structure, the '627 patent teaches that "a distributed trellis encoder . . . generates a plurality of streams of trellis encoded channel symbols in response to respective portions of the input information." (Ex. 1 at 5:1-5). To generate a plurality of streams of trellis encoded channel symbols, the distributed trellis encoder may implement multiple trellis encoding processes. The '627 patent teaches multiple ways to implement these trellis encoding processes. On the one hand, the distributed trellis encoder can implement multiple trellis encoding processes using multiple trellis encoders. (Ex. 1 at 1:59-62, 9:4-8, Fig. 3 (encoders 319α, 319β, and 319γ)). On the other hand, the distributed trellis encoder can implement multiple trellis encoding processes in software, thus functioning as an encoder with a single stage that continually switches the input data to the encoder stage. As a result, the distributed trellis encoder emulates the function of multiple physical encoders. Indeed, the '627

patent specification expressly teaches that "multiple trellis encoders . . . can be realized using a single program routine . . . ." (Ex. 1 at 9:62-63). In either case, once the input information is trellis encoded, the distributed trellis encoder generates channel symbols. Therefore, Rembrandt's structural construction is in accord with the intrinsic record.

All Other Parties' structural construction incorporates limitations from the preferred embodiment. They would have the court limit the structure to "parallel trellis encoders" and an "encoder that generates signal points." As discussed above, nothing in the '627 requires that channel symbols be generated only using *multiple* encoders, let alone "*parallel* trellis encoders." All Other Parties' construction is thus overly limiting and fails to properly encompass all the disclosed embodiments in the specification. *See Data Line Corp. v. Micro Technologies, Inc.*, 813 F.2d 1196, 1201 (Fed. Cir. 1987) (a means-plus-function structure must be "construed to cover both the disclosed structure and equivalents thereof . . ."). Accordingly, All Other Parties' proposed construction should be rejected.

K. "means for interleaving the signal points of said generated channel symbols to form said (a) stream of trellis encoded signal points" (claims 1, 2, 21, and 22)

Rembrandt's Proposed Construction: *interpreted under 35 U.S.C. § 112, ¶ 6.*

Function: *interleaving the signal points of said generated channel symbols to form said (a) stream of trellis encoded signal points.*

Structure: *signal point interleaver and/or a switching circuit, or a processor programmed to interleave the signal points of the trellis encoded channel symbols.*

The parties agree upon function. With regard to structure, if the specification identifies multiple structures that can perform the function, then the construction should encompass each structure. *See Creo Prods., Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1345 (Fed. Cir. 2002). The '627 patent identifies a variety of structures that can perform the recited interleaving function: (1) signal point interleaver (341 or 641) and/or switching circuit (337); or (2) a processor

programmed to interleave the signal points of the trellis encoded channel symbols. (Ex. 1 at 9:52-66). As discussed above, the claims require that interleaving be "carried out in such a way that the signal points of each channel symbol are non-adjacent" and "the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent." (Ex. 1 at Claims 1, 9, 11, 19 and 21; 7:55-64). The specification discloses that (1) signal points belonging to a particular channel symbol are interleaved through use of the signal point interleaver: "signal point interleaver . . . cause[s] the signal points from the same channel symbol to be non-adjacent" (Ex. 1 at 7:10-13, 7:58-64); and (2) signal points of successive channel symbols generated through a given trellis encoder are interleaved through use of a switching circuit: "data word outputs of the trellis encoders are . . . supplied to QAM encoder 324 by switching circuit . . . [to form] interleaved streams of trellis encoded channel symbols" (Ex. 1 at 5:13–28, 7:58-64, 1:59-62). The specification is therefore clear that not only the signal point interleaver, but also the switching circuit is capable of performing the function of interleaving signal points of channel symbols.

All Other Parties continue to incorrectly exclude structural embodiments expressly disclosed in the specification. They would have the court limit the structure to a signal point interleaver with a delay element, but exclude both the switching circuit (337) and "one or more appropriately programmed processors . . . ." (Ex. 1 at 9:60). All Other Parties' construction is thus overly limiting and fails to properly encompass all the disclosed embodiments in the specification. *See Data Line*, 813 F.2d at 1201. Therefore, All Other Parties' construction should be rejected.

L. "means for deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols" (claims 9, 10, 21, and 22)

Rembrandt's Proposed Construction: *interpreted under 35 U.S.C. § 112, ¶ 6.*

Function: *deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols.*

Structure: *signal point deinterleaver and/or a switching circuit, or a processor programmed to deinterleave the interleaved signal points.*

The parties agree on function. Rembrandt agrees that the signal point deinterleaver is one of the corresponding structures to the claimed function. The specification, however, sets forth additional structures that correspond to the claimed function.

The '627 patent identifies a variety of structures that can perform the recited deinterleaving function: (1) a signal point deinterleaver (441 or 741), (Ex. 1 at 5:67-6:11), and/or switching circuit 431 (Ex. 1 at 6:12-6:16); or (2) a processor programmed to deinterleave the interleaved signal points (Ex. 1 at 9:52-66). Yet, All Other Parties' construction is limited to a signal point deinterleaver and a delay element(s). They improperly exclude structural embodiments expressly disclosed in the specification. Thus, their construction is overly limiting and fails to properly encompass all the disclosed embodiments in the specification. *See Data Line*, 813 F.2d at 1201. All Other Parties' construction should be rejected.

V. CONCLUSION

For all of the foregoing reasons, Rembrandt's proposed constructions should be adopted.

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CERTIFICATE OF SERVICE

I, Collins J. Seitz, Jr., hereby certify that on the 4th day of June, 2008, a true copy of the foregoing document was electronically filed with the Clerk of the Court using CM/ECF which will send notification of such filing to the following and the document is available for viewing and downloading from CM/ECF:

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EXHIBIT 1

US005243627A

United States Patent [19]

Betts et al.

[11] Patent Number: 5,243,627

[45] Date of Patent: Sep. 7, 1993

[54] **SIGNAL POINT INTERLEAVING TECHNIQUE**

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[73] Assignee: **AT&T Bell Laboratories**, Murray Hill, N.J.

[21] Appl. No.: **748,594**

[22] Filed: **Aug. 22, 1991**

[51] **Int. Cl.**[5] **H04L 5/12**

[52] **U.S. Cl.** **375/39**; 375/60; 375/99; 371/43

[58] **Field of Search** 375/39, 58, 60, 99; 371/43, 37.5, 2.1, 45; 341/81

[56] **References Cited**

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5,029,185	7/1991	Wei	375/39 X

Primary Examiner—Curtis Kuntz
Assistant Examiner—Tesfaldet Bocure
Attorney, Agent, or Firm—Ronald D. Slusky; Gerard A. deBlasi

[57] **ABSTRACT**

Viterbi decoder performance in a data communication system using 2N-dimensional channel symbols N>1 can be further enhanced by an interleaving technique which uses a distributed trellis encoder in combination with a signal point interleaver.

24 Claims, 4 Drawing Sheets

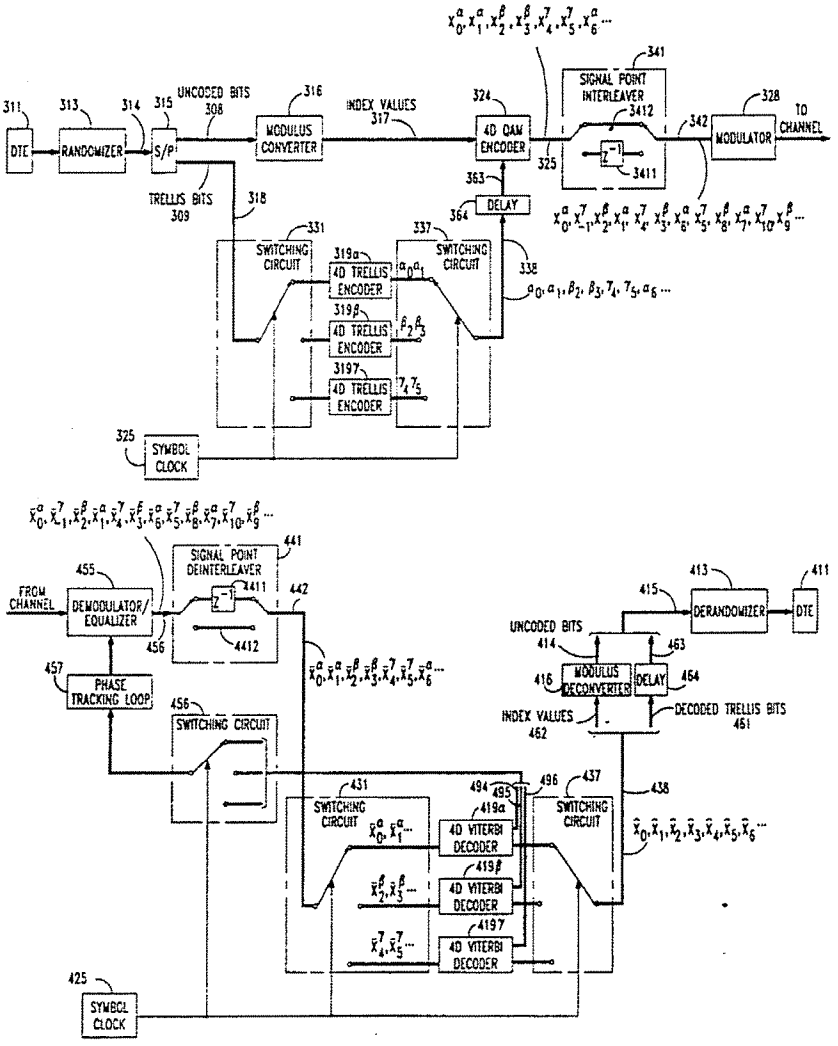


FIG. 1

PRIOR ART

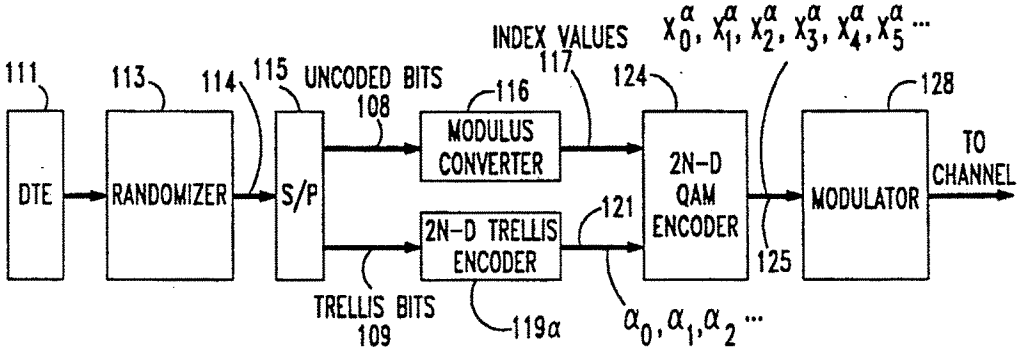


FIG. 2

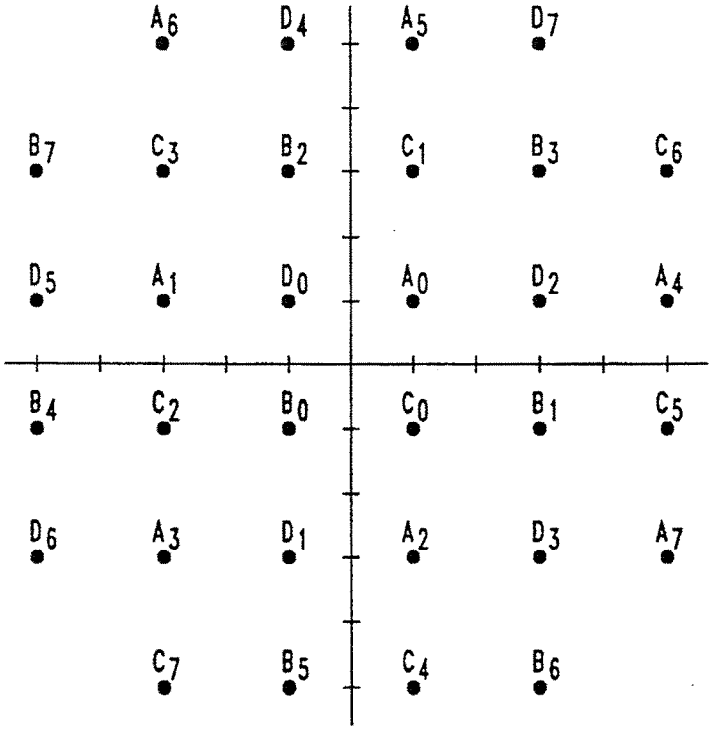
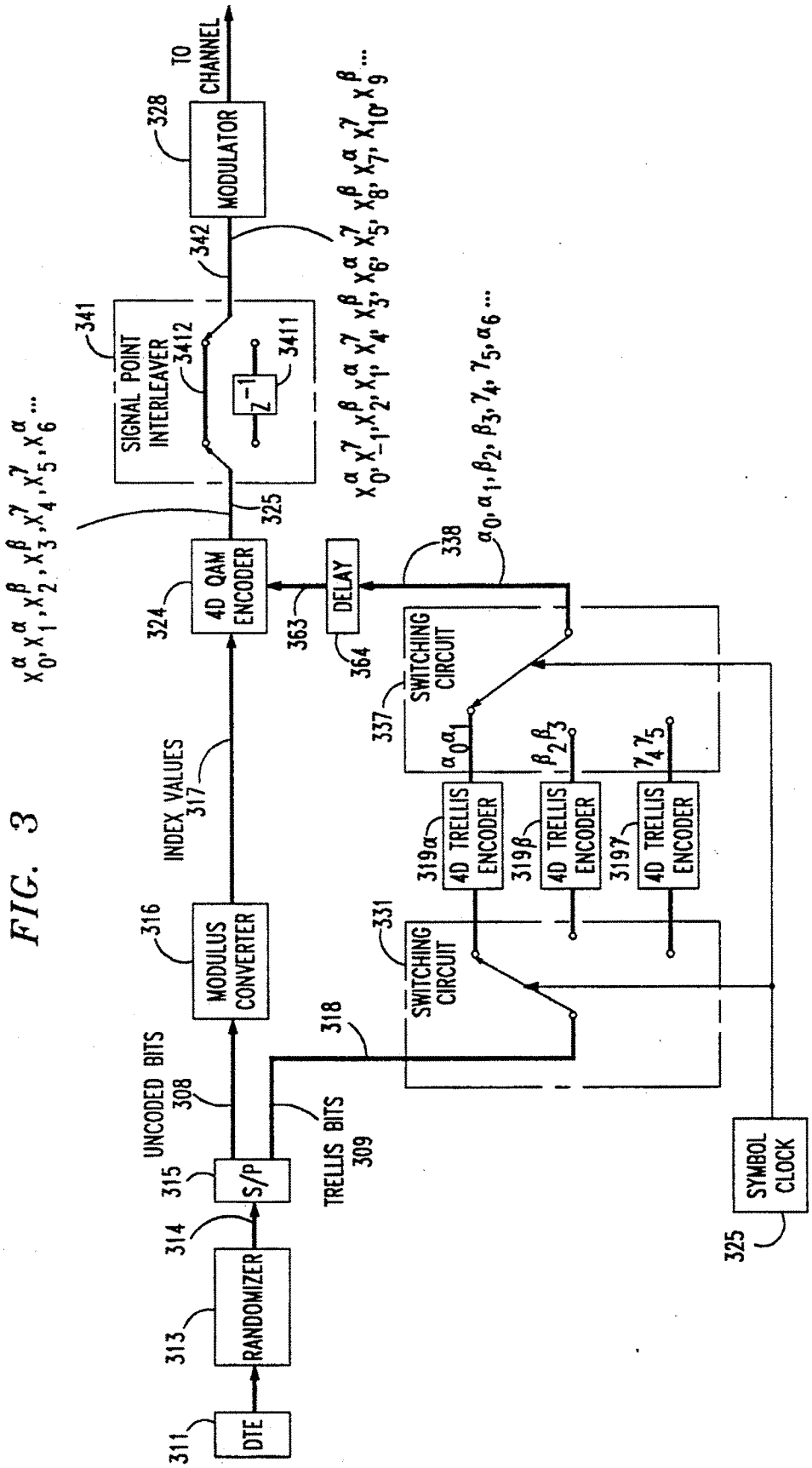


FIG. 3



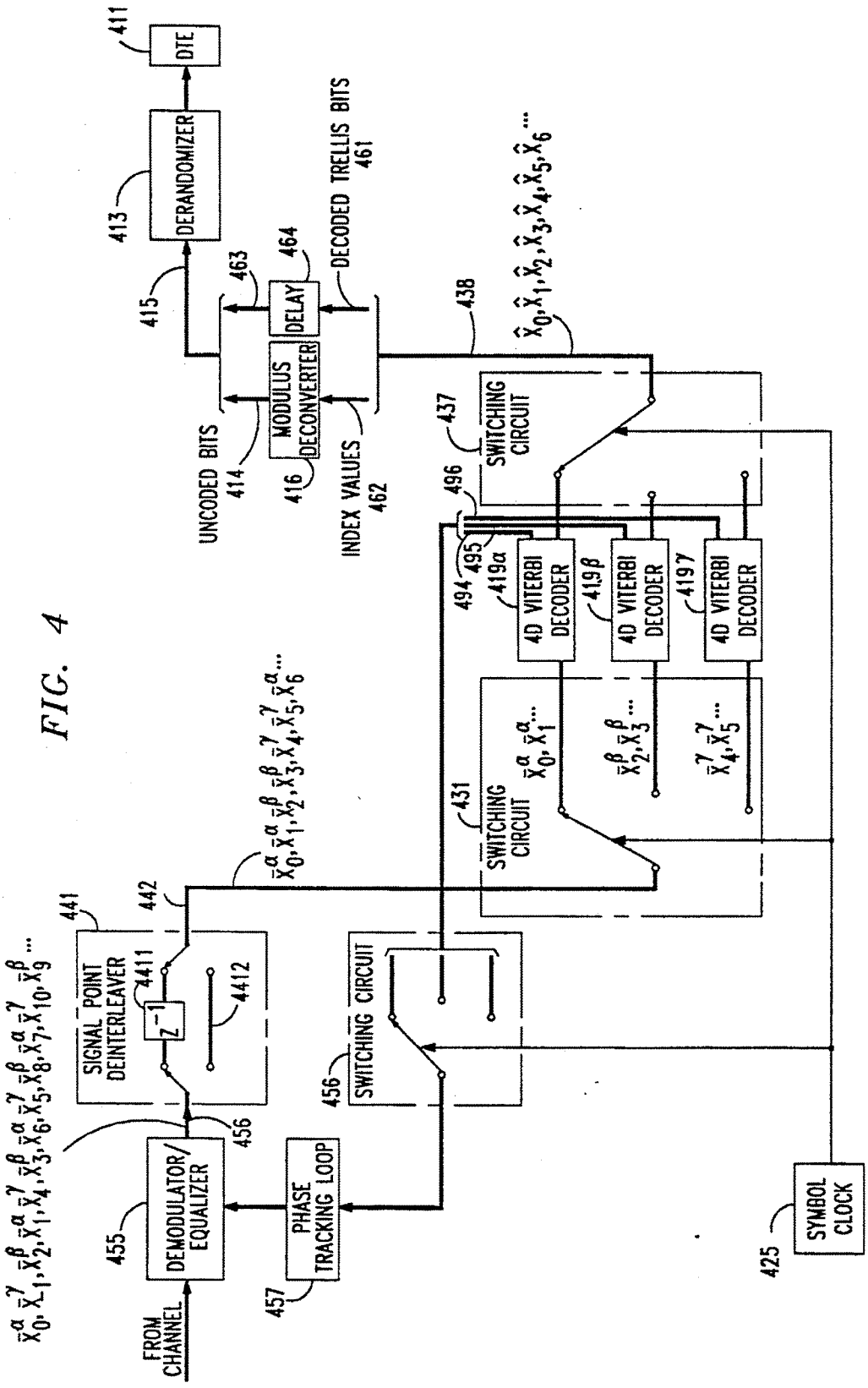

411
DTE
413
DERANDOMIZER
415
463
464
DELAY
DECODED TRELLIS BITS
461
438
UNCODED BITS
414
MODULUS DECONVERTER
416
INDEX VALUES
462
437
SWITCHING CIRCUIT
496
494
495
419α
419β
419γ
4D VITERBI DECODER
4D VITERBI DECODER
4D VITERBI DECODER
431
SWITCHING CIRCUIT
441
SIGNAL POINT DEINTERLEAVER
4411
4412
442
456
SWITCHING CIRCUIT
455
DEMODULATOR/ EQUALIZER
457
PHASE TRACKING LOOP
FROM CHANNEL
425
SYMBOL CLOCK

FIG. 4

FIG. 5

		4D SYMBOL	4D SYMBOL	4D SYMBOL	4D SYMBOL	4D SYMBOL	4D SYMBOL
I	NOT INTERLEAVED ONE TRELLIS STAGE	$X_0^\alpha\ X_1^\alpha$	$X_2^\alpha\ X_3^\alpha$	$X_4^\alpha\ X_5^\alpha$	$X_6^\alpha\ X_7^\alpha$	$X_8^\alpha\ X_9^\alpha$	$X_{10}^\alpha \cdots$
II	NOT INTERLEAVED THREE TRELLIS STAGES	$X_0^\alpha\ X_1^\alpha$	$X_2^\beta\ X_3^\beta$	$X_4^\gamma\ X_5^\gamma$	$X_6^\alpha\ X_7^\alpha$	$X_8^\beta\ X_9^\beta$	$X_{10}^\gamma \cdots$
III	INTERLEAVED ONE TRELLIS STAGE	$X_0^\alpha\ X_{-1}^\alpha$	$X_2^\alpha\ X_1^\alpha$	$X_4^\alpha\ X_3^\alpha$	$X_6^\alpha\ X_5^\alpha$	$X_8^\alpha\ X_7^\alpha$	$X_{10}^\alpha \cdots$
IV	INTERLEAVED TWO TRELLIS STAGES	$X_0^\alpha\ X_{-1}^\beta$	$X_2^\beta\ X_1^\alpha$	$X_4^\alpha\ X_3^\beta$	$X_6^\beta\ X_5^\alpha$	$X_8^\alpha\ X_7^\beta$	$X_{10}^\beta \cdots$
V	INTERLEAVED THREE TRELLIS STAGES	$X_0^\alpha\ X_{-1}^\gamma$	$X_2^\beta\ X_1^\alpha$	$X_4^\gamma\ X_3^\beta$	$X_6^\alpha\ X_5^\gamma$	$X_8^\beta\ X_7^\alpha$	$X_{10}^\gamma \cdots$

FIG. 6

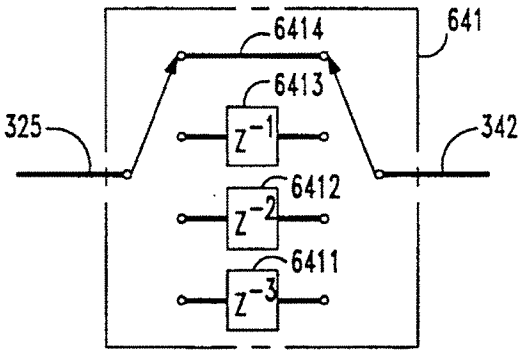
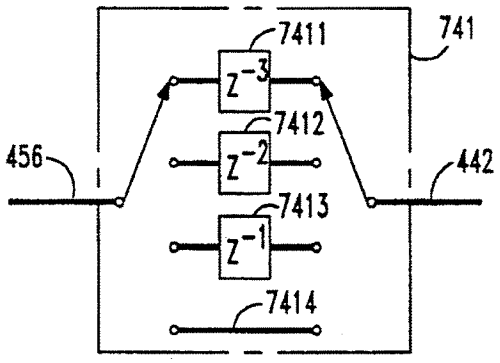


FIG. 7



SIGNAL POINT INTERLEAVING TECHNIQUE

BACKGROUND OF THE INVENTION

The present invention relates to the transmission of digital data over band-limited channels.

Over the years, the requirements of modern-day digital data transmission over band-limited channels—such as voiceband telephone channels—have resulted in a push for higher and higher bit rates. This push has led to the development and introduction of such innovations as adaptive equalization, multi-dimensional signal constellations, echo cancellation (for two-wire applications), and trellis coding. Today, the data rates achieved using these and other techniques are beginning to approach the theoretical limits of the channel.

It has been found that various channel impairments, whose effects on the achievable bit rate were relatively minor compared to, say, additive white Gaussian noise and linear distortion, have now become of greater concern. These include such impairments as nonlinear distortion and residual (i.e., uncompensated-for) phase jitter. Such impairments are particularly irksome in systems which use trellis coding. Indeed, it has been found that the theoretical improvement in Gaussian noise immunity promised by at least some trellis codes is not realized in real-world applications where these impairments are manifest. The principal reason this is so appears to be that the noise components introduced into the received signal samples are such as to worsen the effectiveness of the Viterbi decoder used in the receiver to recover the transmitted data.

U.S. Pat. No. 4,677,625, issued Jun. 30, 1987 to Betts et al, teaches a method and arrangement in which, through the use of a distributed trellis encoder/Viterbi decoder, the effects of many of these impairments can be reduced. The invention in the Betts et al patent recognizes that a part of the reason that the performance of the Viterbi decoder is degraded by these impairments is the fact that the noise components of channel symbols which closely follow one another in the transmission channel are highly correlated for many types of impairments. And it is that correlation which worsens the effect that these impairments have on the Viterbi decoder. Among the impairments whose noise is correlated in this way are impulse noise, phase "hits" and gain "hits." All of these typically extend over a number of adjacent channel symbols in the channel, and thus all result in channel symbol noise components which are highly correlated. The well-known noise enhancement characteristics of linear equalizers also induce correlated noise in adjacent channel symbols, as does uncompensated-for phase jitter. Also, the occurrence of one of the relatively high power points of the signal constellation can, in pulse code modulation (PCM) systems, for example, give rise to noise on adjacent channel symbols which, again, is correlated.

The Betts et al patent addresses this issue by distributing the outgoing data to a plurality of trellis encoders in round-robin fashion and interleaving the trellis encoder outputs on the transmission channel. In the receiver, the stream of received interleaved channel symbols is correspondingly distributed to a plurality of trellis decoders. Since the successive pairs of channel symbols applied to a particular trellis decoder are separated from one another as they traverse the channel, the correlation of the noise components of these channel symbol pairs is reduced from what it would have otherwise been.

SUMMARY OF THE INVENTION

In accordance with the present invention, it has been realized that the Viterbi decoder performance in a data communication system using 2N-dimensional channel symbols can be further enhanced by an interleaving technique which uses, in combination, a) the aforementioned distributed trellis encoder/Viterbi decoder technique and b) a signal point interleaving technique which causes the constituent signal points of the channel symbols to be non-adjacent as they traverse the channel.

In preferred embodiments of the invention, the interleaving is carried out in such a way that every N^{th} signal point in the signal point stream traversing the channel is the N^{th} signal point of a respective one of the channel symbols. This criterion enhances the accuracy with which the phase tracking loop in the receiver performs its function.

Also in preferred embodiments, we have found that the use of three parallel trellis encoders in conjunction with a signal point interleaving regime in which the signal points of each channel symbol are separated from one another by three signaling intervals (bauds) provides an optimum or near-optimum tradeoff between signal point/channel symbol separation and the decoding delay that is caused by the interleaving.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing,

FIG. **1** is a block diagram of the transmitter section of a prior art modem;

FIG. **2** is shows a signal constellation used by the transmitter of FIG. **1**;

FIG. **3** is a block diagram of the transmitter section of a modem employing four-dimensional channel symbols and embodying the principles of the invention;

FIG. **4** is a block diagram of the receiver section of a modem embodying the principles of the invention which processes the received four-dimensional channel symbols generated by the transmitter of FIG. **3**;

FIG. **5** is a signal point timing/sequencing chart helpful in explaining the principles of the present invention;

FIG. **6** is a signal point interleaver which can be used in the transmitter of FIG. **3** to interleave the signal points of eight-dimensional channel symbols; and

FIG. **7** is a signal point deinterleaver which can be used in the receiver of FIG. **4** to deinterleave the signal points of eight-dimensional channel symbols.

DETAILED DESCRIPTION

FIG. **1** depicts the transmitter section of a prior art modem employing a 2N-dimensional signaling scheme, $N \geqq 1$. The modem receives input information in the form of a serial bit stream from data terminal equipment (DTE) **111**—illustratively a host computer. That bit stream is then scrambled, or randomized, by randomizer **113** whose output bits are provided in serial form to serial-to-parallel (S/P) converter **115**.

Serial-to-parallel converter **115**, in turn, provides, during each of a succession of symbol intervals (comprised of N baud intervals), some predetermined number of parallel bits on lead **109** and some number of parallel bits on lead **108**. (It will be appreciated that whenever bits are provided in parallel in the modem, separate leads are required to carry each of the bits.) The bits on lead **109** are applied to trellis encoder **119**α,

and are referred to as the "trellis bits." The bits on lead **108** are applied to modulus converter **116**, and are referred to as the "uncoded bits."

To better understand how trellis encoder **119**α and modulus converter **116** work, reference is made to FIG. **2**, which shows the two-dimensional signal constellation that forms the basis of the 2N-dimensional signaling scheme illustratively used by the modem. This constellation is comprised of 32 signal points, which are divided into four subsets, A through D, each comprised of eight signal points. The eight points of subset A are explicitly labeled as A_0 through A_7. It may be noted that subsets C, B and D can be arrived at by clockwise rotation of subset A by 90, 180 and 270 degrees, respectively. (Conventional differential encoding circuitry within trellis encoder **119**α exploits this symmetry.) For reference, a single signal point of each of those subsets is also shown on FIG. **2**.

Consider, first, the case of N=1, i.e., a two-dimensional signaling scheme. In this case, one trellis bit on lead **109** would be expanded to two bits by trellis encoder **119**α on lead **121**. The four possible values of those three bits **00**, **01**, **10**, and **11** identify subsets A, B, C and D, respectively. The successive 2-bit words on lead **121** are represented as α_n, n=0,1,2. . . , where n is an index that advances at the baud rate. At the same time, three parallel bits would be provided on lead **108**. These are converted by modulus converter **116** into an index having a value within the range (decimal) 0 to 7. The index value, represented in binary form on lead **117**, selects a particular signal point from the subset identified on lead **121**. Thus if lead **121** carries the two bits **00** while lead **117** carries the three bits **001**, then signal point A_1 of the FIG. **2** constellation has been selected. The words on leads **117** and **121** are applied to QAM encoder **124** which generates, on lead **125**, values representing the I (in-phase) and Q (quadrature-phase) components of signal point A_1. The signal point generated on lead **125** in the n^{th} baud interval is denoted X_n^{α}, which is passed on to modulator **128** to generate a pass-band line signal which is applied to the communication channel. The superscript, α, indicates that the trellis encoder that was used to identify the subset for any particular signal point was trellis encoder **119**α. That is, of course, a trivial notation as far as FIG. **1** goes inasmuch as trellis encoder **119**α is the only trellis encoder in the modem. However, it is useful to introduce this notation because more than one trellis encoder stage is used in preferred embodiments of modems incorporating the principles of the present invention as shown in later FIGS.

In the case of N>1, the operation is similar. Now, however, the words on lead **109** are used by trellis encoder **119**α to sequentially identify on lead **121**N subsets, while the words on lead **108** are used to generate N corresponding index values on lead **117**. The N signal points identified in this way are the component signal points of a 2N-dimensional channel symbol, the first such symbol being comprised of the signal points X_0^{α}, . . . $X_{(N-1)}^{\alpha}$. For example, a modem in which the transmitter of FIG. **1** could be used may be a 14,400 bit per second modem using four-dimensional coding (i.e., N=2) and a baud rate of 3200. In this case, nine bits from S/P converter **115** are used for each four-dimensional symbol. Specifically, three parallel bits on lead **109** are expanded into four bits on lead **121** to identify a pair of subsets while six bits on lead **108** are used to select particular signal points from those two subsets. Those two signal points are thereupon communicated over the channel by QAM encoder **124** and modulator **128** as described above.

Note that, implementationally, the 2N-dimensional channel symbol is generated by having the trellis encoder identify, interdependently, N subsets of the two-dimensional constellation of FIG. **2**, then select a two-dimensional signal point from each of the subsets thus identified. The concatenation of the N two-dimensional signal points thus selected is the desired 2N-dimensional channel symbol. This process, however, can be understood as involving the direct selection of a 2N-dimensional channel symbol. Viewed in this context, the set of all possible combinations of N of the two-dimensional subsets identified by N successive trellis encoder outputs can be understood to be a set of 2N-dimensional subsets of a 2N-dimensional constellation, the latter being comprised of all possible combinations of N of the signal points of the two-dimensional constellation. A succession of N outputs from the trellis encoder identifies a particular one of the 2N-dimensional subsets and a succession of N outputs from the modulus converter selects a particular 2N-dimensional signal point from the identified 2N-dimensional subset.

Modulus converter **116** is illustratively of the type disclosed in co-pending, commonly-assigned U.S. patent application Ser. No. 588,658 filed Sep. 26, 1990 and allowed on May 21, 1991, hereby incorporated by reference. Modulus converter **116** provides the modem with the ability to support data transmission at various different bit rates. Assume, for example, that the rate at which bits are provided by DTE **111** decreases. The serial-to-parallel converter will continue to provide its outputs on leads **108** and **109** at the same baud rate as before. However, the upper limit of the range of index values that are provided by modulus converter **116** on lead **117** will be reduced, so that, effectively, each of the four subsets A through D, instead of having eight signal points, will have some smaller number. Conversely if the rate at which bits are provided by DTE **111** should increase over that originally assumed, the upper limit of the range of index values, and thus the number of parallel bits, that appear on lead **117** will be increased beyond eight and the constellation itself will be expanded to accommodate the larger number of signal points thus being selected. As an alternative to using a modulus converter, fractional bit rates can be supported using, for example, the technique disclosed in L. Wei, "Trellis-Coded Modulation with Multidimensional Constellations," *IEEE Trans. on Communication Theory*, Vol. IT-33, No. 4, July 1987, pp. 483–501.

Turning now to FIG. **3**, the transmitter portion of a modem embodying the principles of the invention is shown. This embodiment illustratively uses the aforementioned four-dimensional, i.e., N=2, signaling scheme. Many of the components are similar to those shown in FIG. **1**. Thus, in particular, the transmitter of FIG. **3**—which receives its input information in the form of a stream of input bits from DTE **311**—includes randomizer **313**, which supplies its output, on lead **314**, to S/P converter **315**. The latter outputs uncoded bits to modulus converter **316**. The transmitter further includes four-dimensional QAM encoder **324** and modulator **328**. The trellis bits, on lead **309**, are provided not to a standard single trellis encoder, but to a distributed trellis encoder comprised of three trellis encoder stages: trellis encoder stage **319**α, trellis encoder stage **319**β, and trellis encoder stage **319**γ.

Such a distributed trellis encoder, which is described in the aforementioned Betts et al patent, generates a plurality of streams of trellis encoded channel symbols in response to respective portions of the input information. Specifically, a three-bit word on lead **309** is supplied to trellis encoder stage **319**α. The next three-bit word on lead **309** is supplied to trellis encoder stage **319**β. The next three-bit word is supplied to trellis encoder stage **319**γ, and then back to trellis encoder stage **319**α. This distribution of the trellis bits to the various trellis encoder stages is performed by switching circuit **331** operating under the control of symbol clock **325**. The initial data word outputs of the trellis encoders are subset identifiers α_0 and α_1 for encoder stage **319**α, β_2 and β_3 for encoder stage **319**β, and γ_4 and γ_5 for encoder stage **319**γ, followed by α_6 and α_7 for encoder stage **319**α, and so forth. These are supplied to four-dimensional QAM encoder **324** by switching circuit **337**—also operating under the control of symbol clock **325**—on lead **338** through a one-symbol delay **364** and lead **363**, in order to compensate for a one-symbol delay caused by modulus converter **316**. Thus, the stream of subset identifiers on lead **338** is $\alpha_0, \alpha_1, \beta_2, \beta_3, \gamma_4, \gamma_5, \alpha_6 \ldots$. Using the notation introduced above, then, the output of encoder **324** on lead **325** is the stream of signal points $X_0^\alpha, X_1^\alpha, X_2^\beta, X_3^\beta, X_4^\gamma, X_5^\gamma, X_6^\alpha \ldots$, which is comprised of three interleaved streams of trellis encoded channel symbols, these streams being $X_0^\alpha, X_1^\alpha, X_6^\alpha, X_7^\alpha, X_{12}^\alpha \ldots$; $X_2^\beta, X_3^\beta, X_8^\beta, X_9^\beta, X_{14}^\beta \ldots$; and $X_4^\gamma, X_5^\gamma, X_{10}^\gamma, X_{11}^\gamma, X_{16}^\gamma \ldots$. These, in turn, are supplied, in accordance with the invention, to signal point interleaver **341** which applies alternate ones of the signal points applied thereto to lead **3412**—which signal points appear immediately at the interleaver output on lead **342**—and to one-symbol (Z^{-1}) delay element **3411**, which appear on lead **342** after being delayed therein by one symbol interval. The resulting interleaved stream of trellis encoded signal points is $X_0^\alpha, X_{-1}^\gamma, X_2^\beta, X_1^\alpha, X_4^\gamma, X_3^\beta, X_6^\alpha, X_5^\gamma, X_8^\beta, X_7^\alpha, X_{10}^\gamma, X_9^\beta \ldots$ (the signal point X_{-1}^γ being, of course, the signal point applied to interleaver **341** just ahead of signal point X_0^α).

A discussion and explanation of how the interleaving just described is advantageous is set forth hereinbelow. In order to fully set the stage for that explanation, however, it will be first useful to consider the receiver section of a modem which receives the interleaved signal point stream.

Thus referring to FIG. **4**, the line signal transmitted by the transmitter of FIG. **3** is received from the channel and applied to demodulator/equalizer **455** which, in conventional fashion—including an input from phase tracking loop **457**—generates a stream of outputs on lead **456** representing the demodulator/equalizer's best approximation of the values of the I and Q components of the signal points of the transmitted interleaved signal point stream. These outputs are referred to herein as the "received signal points." (Due to distortion and other channel impairments that the demodulator/equalizer is not able to compensate for, the I and Q components of the received signal points, instead of having exact integer values, can have any value. Thus a transmitted signal point having coordinates (3, −5) may be output by the demodulator/equalizer as the received signal point (2.945, −5.001).) The stream of received signal points on lead **456** is denoted $\overline{X}_0^\alpha, \overline{X}_{-1}^\gamma, \overline{X}_2^\beta, \overline{X}_1^\alpha, \overline{X}_4^\gamma, \overline{X}_3^\beta, \overline{X}_6^\alpha, \overline{X}_5^\gamma, \overline{X}_8^\beta, \overline{X}_7^\alpha, \overline{X}_{10}^\gamma, \overline{X}_9^\beta \ldots$.

The successive received signal points are deinterleaved in signal point deinterleaver **441**, which provides the opposite function to interleaver **341** in the transmitter. The output of deinterleaver **441** on lead **442** is thus $\overline{X}_0^\alpha, \overline{X}_1^\alpha, \overline{X}_2^\beta, \overline{X}_3^\beta, \overline{X}_4^\gamma, \overline{X}_5^\gamma, \overline{X}_6^\alpha, \ldots$, etc. (Although not explicitly shown in the drawing, the same well-known techniques used in modems of this general kind to identify within the stream of received signal points the boundaries between successive symbols is used to synchronize the operation of signal point deinterleaver **441** to ensure that received signal points $\overline{X}_0^\alpha, \overline{X}_2^\beta, \overline{X}_4^\gamma \ldots$ are applied to delay element **4411** while received signal points $\overline{X}_1^\alpha, \overline{X}_3^\beta, \overline{X}_5^\gamma \ldots$ are applied to lead **4412**.)

The received signal points on lead **442** are then distributed by switching circuit **431** under the control of symbol clock **425** to a distributed Viterbi decoder comprised of 4D Viterbi decoder stages **419**α, **419**β and **419**γ. Specifically, received signal points $\overline{X}_0^\alpha$ and $\overline{X}_1^\alpha$ are applied to decoder stage **419**α; received signal points $\overline{X}_2^\beta$ and $\overline{X}_3^\beta$ are applied to decoder stage **419**β; and received signal points $\overline{X}_4^\gamma$ and $\overline{X}_5^\gamma$ are applied to decoder stage **419**γ. The outputs of the three decoder stages are then combined into a serial stream on lead **438** by switching circuit **437**, also operating under the control of symbol clock **425**. Those outputs, representing decisions as to the values of the transmitted signal points, are denoted $\hat{X}_0, \hat{X}_1, \hat{X}_2, \hat{X}_3, \hat{X}_4, \hat{X}_5, \hat{X}_6, \ldots$, the α, β and γ superscripts no longer being needed.

In conventional fashion, the bits that represent each of the decisions on lead **438** can be divided into bits that represent a) the trellis bits that appeared on transmitter lead **309** and b) the index values that appeared on transmitter lead **317**. Those two groups of bits are provided in the receiver on leads **461** and **462**, respectively. The latter group of bits are deconverted by modulus deconverter **416** (also disclosed in the aforementioned '658 patent application) back to uncoded bit values on lead **414**. The operation of the modulus deconverter imparts a one-symbol delay to the bits on lead **414**. Accordingly, the bits on lead **461** are caused to be delayed by one symbol by delay element **464**. The resulting combined bits on lead **415** thus represent the stream of bits that appeared at the output of randomizer **313** in the transmitter. These are derandomized in the receiver by derandomizer **413** and the resulting derandomized bit stream is applied to DTE **411** which may be, for example, a computer terminal.

Referring to FIG. **5**, one can see the improvement that is achieved by the present invention.

Line I shows the stream of output signal points generated and launched into the channel using one stage of trellis encoding and no signal point interleaving. This is, of course, the prior art arrangement shown in FIG. **1**. Line II shows the effect of providing a three-stage distributed trellis encoder but still no signal point interleaving. This is the arrangement shown in the aforementioned Betts et al patent. Note that the signal points of each channel symbol operated on by a particular trellis encoder stage are adjacent in the output signal point stream. For example, the second signal point of the symbol $X_0^\alpha X_1^\alpha$—namely signal point X_1^α—is separated by five baud intervals from the first (closer) signal point of the symbol $X_6^\alpha X_7^\alpha$—namely signal point X_6^α. As noted earlier, such separation is advantageous because the channel symbols which are processed one after the other in a particular Viterbi decoder stage have noise components which are not highly correlated.

Note, however, that the individual signal points of each channel symbol, e.g., X_0^α and X_1^α, are adjacent to

one another as they pass through the channel; and since all the signal points of a channel symbol must be processed serially in the same Viterbi decoder stage, this means that the Viterbi decoder must process adjacent signal points that have highly correlated noise components.

It is to this end that signal point interleaver **341** is included within the transmitter in accordance with the invention. Firstly, it may be noted from Line III that using the signal point interleaver without the distributed trellis encoder—an arrangement not depicted in the drawing—will, advantageously, cause the signal points from the same channel symbol to be non-adjacent. Moreover, there is further advantage in that a pair of channel symbols processed serially by Viterbi decoder stage **419**α traverses the channel separated by five baud intervals rather than three, thereby providing greater decorrelation of the noise components thereof. Compare, for example, the span of baud intervals occupied by signal points X_0^{α} and X_1^{α}, X_2^{α} and X_3^{α} in Line I and the span of baud intervals occupied by the same signal points in Line III. Disadvantageously, however, the use of a single trellis encoding stage brings back the problem that the distributed trellis encoder solves, as described above. Thus, for example, although signal points X_0^{α} and X_1^{α}, which are from the same channel symbol, are separated from one another when traversing the channel, we find that, disadvantageously, signal points X_2^{α} and X_1^{α}, which are signal points from two different channel symbols which will be processed serially by the Viterbi decoder, traverse the channel adjacent to one another.

Line IV shows that using the signal point interleaver with a two-stage trellis encoder—also an arrangement not depicted in the drawing—provides some improvement. Firstly, it may be noted that, as in Line III, signal points from the same channel symbol remain separated by three baud intervals. Additionally, pairs of channel symbols processed sequentially by a given Viterbi decoder stage—such as the channel symbols comprised of signal points X_0^{α} and X_1^{α}, X_4^{α} and X_5^{α}—are still non-adjacent and, indeed, are now separated by seven baud intervals, which is even greater than the separation of five baud intervals provided in Line III. Moreover, certain signal points that traverse the channel adjacent to one another and which are from channel symbols which would have been decoded sequentially in the one-trellis-encoding-stage case are, in the two-trellis-encoding-stage case of Line IV, processed by different Viterbi decoding stages. Signal points X_2^{β} and X_1^{α} are such a pair of signal points. Note, however, that, disadvantageously, signal points X_1^{α} and X_4^{α} traverse the channel serially, and are from channel symbols which are serially processed by the "α" Viterbi decoder stage.

Referring, however, to Line V, which depicts the stream of signal points output by the transmitter of FIG. **3**, it will be seen that, in accordance with the invention, there is still a non-adjacency—indeed, a separation of at least three baud intervals—between a) the signal points which belong to any particular channel symbol (and which, therefore, are processed serially by a particular Viterbi decoder stage) and b) the signal points which belong to channel symbols which are processed serially by a Viterbi decoder stage. Thus, for example, signal points X_1^{α} and X_4^{γ} are now processed by different Viterbi decoder stages. Moreover, pairs of channel symbols processed sequentially by a given Viterbi decoder stage—such as the channel symbols comprised of signal points X_0^{α} and X_1^{α}, X_6^{α} and X_7^{α}—are now separated by none baud intervals.

Using more than three trellis encoder stages in the distributed trellis encoder and/or a signal point interleaver that separates signal points from the same channel symbol by more than three baud intervals would provide even greater separation and could, therefore, potentially provide even greater improvement in Viterbi decoding. However, such improvement comes at a price—that price being increased decoding delay—particularly as the number of trellis encoders is increased beyond three. An engineering trade-off can be made, as suits any particular application.

Moreover, it is desirable for the signal point interleaver to provide a sequence in which every N^{th} signal point in the interleaved signal point stream is the N^{th} signal point of a channel symbol. (The reason this is desirable is described in detail hereinbelow.) In the case of an N=2, four-dimensional signaling scheme, this means that every second, that is "every other," signal point in the interleaved stream is the second signal point of the channel symbol from which it comes. In the case of an N=4, eight-dimensional signaling scheme, this means that every fourth signal point in the interleaved stream is the fourth signal point of the channel symbol from which it comes. Indeed, this criterion is in fact satisfied in the embodiment of FIG. **3**. Note that each one of signal points X_0^{α}, X_2^{β}, X_4^{γ}, X_6^{α}, . . . , which appear as every other signal point in the interleaved stream, is the second signal point of one of the four-dimensional channel symbols. Note that not all rearrangements of the signal points will, in fact, satisfy this criterion, such as, if the two signal points of a channel symbol are separated by two, rather than three, baud intervals.

Satisfying the above criterion is advantageous because it enhances the accuracy with which phase tracking loop **457** performs its function. This is so because the arrival of an N^{th} signal point of a given symbol means that all the signal points comprising that channel symbol have arrived. This, in turn, makes it possible to form a decision as to the identity of that channel symbol by using the minimum accumulated path metric in the Viterbi decoder stages. (Those decisions are fed back to the tracking loop by decoder stages **419**α, **419**β **419**γ on leads **494**, **495** and **496**, respectively, via switching circuit **456**.) Without having received all of the signal points of a channel symbol, one cannot take advantage of the accumulated path metric information but, rather, must rely on the so-called raw sliced values, which is less accurate. By having every N^{th} signal point in the interleaved stream be the N^{th} signal point of a channel symbol, we are guaranteed that the time between adjacent such path metric "decisions" supplied to the phase tracking loop is, advantageously, never more than N baud intervals.

The foregoing merely illustrates the principles of the invention. Thus although the illustrative embodiment utilizes a four-dimensional signaling scheme, the invention can be used with signaling schemes of any dimensionality. In the general, 2N-dimensional, case each stage of the distributed trellis encoder would provide N two-dimensional subset identifiers to switching circuit **337** before the latter moves on to the next stage. And, of course, each stage of the distributed Viterbi decoder would receive N successive received signal points. The distributed trellis encoder and distributed Viterbi decoder can, however, continue to include three trellis

encoders and still maintain, independent of the value of N, a separation of three baud intervals in the channel between signal points that are from channel symbols that are adjacent in the trellis encoder. If a greater separation of such signal points is desired, more stages can be added to the distributed trellis encoder/Viterbi decoder, just as was noted above for the four-dimensional case. However, when dealing with 2N-dimensional signaling where $N>2$, it is necessary to add additional delay elements to the signal point interleaver/deinterleaver in order to maintain a three-baud-interval separation among the signal points from any given channel symbol.

Consider, for example, the case of $N=4$, i.e., an eight-dimensional case. Looking again at FIG. **3**, the three (8D) stages of the distributed trellis encoder would generate the three streams of subset identifiers $\alpha_0\,\alpha_1\,\alpha_2\,\alpha_3\,\alpha_{12}\ldots$, $\beta_4\,\beta_5\,\beta_6\,\beta_7\,\beta_{16}\ldots$, and $\gamma_8\,\gamma_9\,\gamma_{10}\,\gamma_{11}\,\gamma_{20}\ldots$, respectively. This would lead to the following stream of signal points of eight-dimensional trellis encoded channel symbols at the output of the QAM encoder on lead **325**: $X_0^{\alpha}\,X_1^{\alpha}\,X_2^{\alpha}\,X_3^{\alpha}\,X_4^{\beta}\,X_5^{\beta}\,X_6^{\beta}\,X_7^{\beta}\,X_8^{\gamma}\,X_9^{\gamma}X_{10}^{\gamma}\,X_{11}^{\gamma}\,X_{12}^{\alpha}\ldots$ Signal point interleaving could be carried out by substituting signal point interleaver **641** of FIG. **6** for interleaver **341**. Interleaver **641**, in addition to direct connection **6414**, includes one-, two-, and three-symbol delay elements **6413**, **6412** and **6411**, respectively.

The signal points on lead **325**, after passing through interleaver **641**, would appear on lead **342** in the following order: $X_0^{\alpha}\,X_{-3}^{\gamma}\,X_{-6}^{\beta}\,X_{-9}^{\alpha}\,X_4^{\beta}\,X_1^{\alpha}\,X_{-2}^{\gamma}\,X_{-5}^{\beta}\,X_8^{\gamma}\,X_5^{\beta}\,X_2^{\alpha}\,X_{-1}^{\gamma}\,X_{12}^{\alpha}\,X_9^{\gamma}\,X_6^{\beta}\,X_3^{\alpha}\,X_{16}^{\beta}\,X_{13}^{\alpha}\,X_{10}^{\gamma}\,X_7^{\beta}\ldots$ where signal points with negative subscripts are, of course, signal points that arrived before signal point X_0^{α} and were already stored in the delay elements **6411**, **6412** and **6413**. Examination of this signal point stream will reveal that there is either a three- or five-baud separation between signal points of channel symbols that are processed sequentially by the same trellis encoder stage, e.g., X_3^{α} and X_{12}^{α}; that adjacent signal points of any one channel symbol, e.g., X_0^{α} and X_1^{α}, are separated by five baud intervals; and that the four signal points comprising any particular one channel symbol are separated by fifteen baud intervals.

FIG. **7** shows the structure of a deinterleaver **741** that could be used in the receiver of FIG. **4** in place of deinterleaver **441** in order to restore the signal points of the eight-dimensional channel symbols to their original order. This structure, which is the inverse of interleaver **641**, includes delay stages **7411**, **7412** and **7413**, as well as direct connection **7414**.

It will be appreciated that, although various components of the modem transmitter and receiver are disclosed herein for pedagogic clarity as discrete functional elements and indeed—in the case of the various switching circuits—as mechanical elements, those skilled in the art will recognize that the function of any one or more of those elements could be implemented with any appropriate available technology, including one or more appropriately programmed processors, digital signal processing (DSP) chips, etc. For example, multiple trellis encoders and decoders can be realized using a single program routine which, through the mechanism of indirect addressing of multiple arrays within memory, serves to provide the function of each of the multiple devices.

It will thus be appreciated that those skilled in the art will be able to devise numerous arrangements which, although not explicitly shown or described herein, embody the principles of the invention and are within its spirit and scope.

We claim:

1. Apparatus for forming a stream of trellis encoded signal points in response to input information, said apparatus comprising

means for generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said input information, each of said channel symbols being comprised of a plurality of signal points, and

means for interleaving the signal points of said generated channel symbols to form said stream of trellis encoded signal points, said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points.

2. The apparatus of claim **1** wherein said means for generating generates three of said streams of trellis encoded channel symbols, and wherein said means for interleaving causes there to be interleaved between each of the signal points of each channel symbol at least two signal points from other channel symbols of said streams of trellis encoded channel symbols.

3. The apparatus of claim **1** wherein said channel symbols are 2N-dimensional channel symbols, $N>1$, and wherein said means for interleaving causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

4. The apparatus of claim **2** wherein said channel symbols are 2N-dimensional channel symbols, $N>1$, and wherein said means for interleaving causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

5. A modem comprising

means for receiving a stream of input bits,

means for dividing said stream of input bits into a stream of uncoded bits and a plurality of streams of trellis bits,

means for independently trellis encoding each of said plurality of streams of trellis bits to generate respective streams of data words each identifying one of a plurality of predetermined subsets of the channel symbols of a predetermined 2N-dimensional constellation, N being an integer greater than unity, each of said channel symbols being comprised of a plurality of signal points,

means for selecting an individual channel symbol from each identified subset in response to said stream of uncoded bits to form a stream of channel symbols, and

means for generating a stream of output signal points, said signal point stream being comprised of the signal points of the selected channel symbols, the signal points of said signal point stream being sequenced in such a way that signal points that are either a) part of the same channel symbol, or b) part of channel symbols that are adjacent to one another in said channel symbol stream, are separated in said output stream by at least one other signal point.

6. The apparatus of claim **5** wherein said trellis encoding means includes a plurality of trellis encoder stage

means for trellis encoding respective ones of said streams of trellis bits.

7. The apparatus of claim 5 wherein said means for selecting includes means for modulus converting said stream of uncoded bits.

8. The apparatus of claim 5 wherein said channel symbols are 2N-dimensional channel symbols, N>1, and wherein said means for generating causes every N^{th} signal point in said stream of output signal points to be the N^{th} signal point of a respective one of said channel symbols.

9. Receiver apparatus for recovering information from a received stream of trellis encoded signal points, said signal points having been transmitted to said receiver apparatus by transmitter apparatus which generates said signal points by generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said information, each of said channel symbols being comprised of a plurality of signal points, and by interleaving the signal points of said generated channel symbols to form said stream of trellis encoded signal points, said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points,

said receiver apparatus comprising

means for deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols, and

a distributed Viterbi decoder for recovering said information from the deinterleaved signal points.

10. The apparatus of claim 9 further comprising

a phase tracking loop, and

means for adapting the operation of said phase tracking loop in response to minimum accumulated path metrics in said distributed Viterbi decoder.

11. A method for forming a stream of trellis encoded signal points in response to input information, said method comprising the steps of

generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said input information, each of said channel symbols being comprised of a plurality of signal points, and

interleaving the signal points of said generated channel symbols to form said stream of trellis encoded signal points, said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points.

12. The method of claim 11 wherein said generating step generates three of said streams of trellis encoded channel symbols, and wherein said interleaving step causes there to be interleaved between each of the signal points of each channel symbol at least two signal points from other channel symbols of said streams of trellis encoded channel symbols.

13. The method of claim 11 wherein said channel symbols are 2N-dimensional channel symbols, N>1, and wherein said interleaving step causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

14. The method of claim 12 wherein said channel symbols are 2N-dimensional channel symbols, N>1, and wherein said interleaving step causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

15. A method for use in a modem, said method comprising the steps of

receiving a stream of input bits,

dividing said stream of input bits into a stream of uncoded bits and a plurality of streams of trellis bits,

independently trellis encoding each of said plurality of streams of trellis bits to generate respective streams of data words each identifying one of a plurality of predetermined subsets of the channel symbols of a predetermined 2N-dimensional constellation, N being an integer greater than unity, each of said channel symbols being comprised of a plurality of signal points,

selecting an individual channel symbol from each identified subset in response to said stream of uncoded bits to form a stream of channel symbols, and

generating a stream of output signal points, said signal point stream being comprised of the signal points of the selected channel symbols, the signal points of said signal point stream being sequenced in such a way that signal points that are either a) part of the same channel symbol, or b) part of channel symbols that are adjacent to one another in said channel symbol stream, are separated in said output stream by at least one other signal point.

16. The method of claim 15 wherein in said trellis encoding step a plurality of trellis encoder stages trellis encode respective ones of said streams of trellis bits.

17. The method of claim 15 wherein said selecting step includes the step of modulus converting said stream of uncoded bits.

18. The method of claim 15 wherein said channel symbols are 2N-dimensional channel symbols, N>1, and wherein said generating step causes every N^{th} signal point in said stream of output signal points to be the N^{th} signal point of a respective one of said channel symbols.

19. A method for use in a receiver to recover information from a received stream of trellis encoded signal points, said signal points having been transmitted to said receiver apparatus by a method which includes the steps of

generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said information, each of said channel symbols being comprised of a plurality of signal points, and

interleaving the signal points of said generated channel symbols to form said stream of trellis encoded signal points, said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points,

said method comprising the steps of

deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols, and

using a distributed Viterbi decoder to recover said information from the deinterleaved signal points.

20. The method of claim **19** wherein said receiver includes a phase tracking loop and wherein said method comprises the further step of adapting the operation of said phase tracking loop in response to minimum accumulated path metrics in said distributed Viterbi decoder.

21. Data communication apparatus comprising

means for receiving input information,

means for generating a plurality of streams of trellis encoded channel symbols in response to respective portions of said input information, each of said channel symbols being comprised of a plurality of signal points,

means for interleaving the signal points of said generated channel symbols to form a stream of trellis encoded signal points, said interleaving being carried out in such a way that the signal points of each channel symbol are non-adjacent in said stream of trellis encoded signal points and such that the signal points of adjacent symbols in any one of said channel symbol streams are non-adjacent in said stream of trellis encoded signal points,

means for applying the stream of trellis encoded signal points to a transmission channel,

means for receiving the stream of trellis encoded signal points from the channel,

means for deinterleaving the interleaved signal points to recover said plurality of streams of trellis encoded channel symbols, and

a distributed Viterbi decoder for recovering said information from the deinterleaved signal points.

22. The apparatus of claim **21** wherein said means for generating generates three of said streams of trellis encoded channel symbols, and wherein said means for interleaving causes there to be interleaved between each of the signal points of each channel symbol at least two signal points from other channel symbols of said streams of trellis encoded channel symbols.

23. The apparatus of claim **21** wherein said channel symbols are 2N-dimensional channel symbols, $N>1$, and wherein said means for interleaving causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

24. The apparatus of claim **22** wherein said channel symbols are 2N-dimensional channel symbols, $N>1$, and wherein said means for interleaving causes every N^{th} signal point in said interleaved signal point stream to be the N^{th} signal point of a respective one of said channel symbols.

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EXHIBIT 2

United States Patent [19]

Betts et al.

[11] **Patent Number: 4,677,625**

[45] **Date of Patent: Jun. 30, 1987**

[54] **DISTRIBUTED TRELLIS ENCODER**

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[73] Assignee: **Paradyne Corporation**, Largo, Fla.

[21] Appl. No.: **707,084**

[22] Filed: **Mar. 1, 1985**

[51] **Int. Cl.**[4] **G06F 11/10**; H03M 13/22

[52] **U.S. Cl.** ..... **371/43**; 340/347 DD; 371/2; 375/26; 375/39

[58] **Field of Search** ..... 340/347 DD; 371/43–45, 371/2; 360/39–42; 375/25, 34, 39

[56] **References Cited**

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4,087,787	5/1978	Acampora	371/43
4,240,156	12/1980	Doland	371/43
4,500,994	2/1985	McCallister et al.	371/43
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Primary Examiner—T. J. Sloyan

Attorney, Agent, or Firm—Kane, Dalsimer, Sullivan, Kurucz

[57] **ABSTRACT**

In the transmitter of a data communication system using QAM, a plurality of trellis coders with delay units are used for forward error correction. The output of each encoder is modulated using QAM to generate sequential baud signal elements. The redundant data bits generated are distributed between several non-consecutive bauds. Likewise, at the receiver a plurality of distributed convolutional decoders are utilized to decode the received signal element. The distributed trellis decoder is self-synchronizing.

11 Claims, 4 Drawing Figures

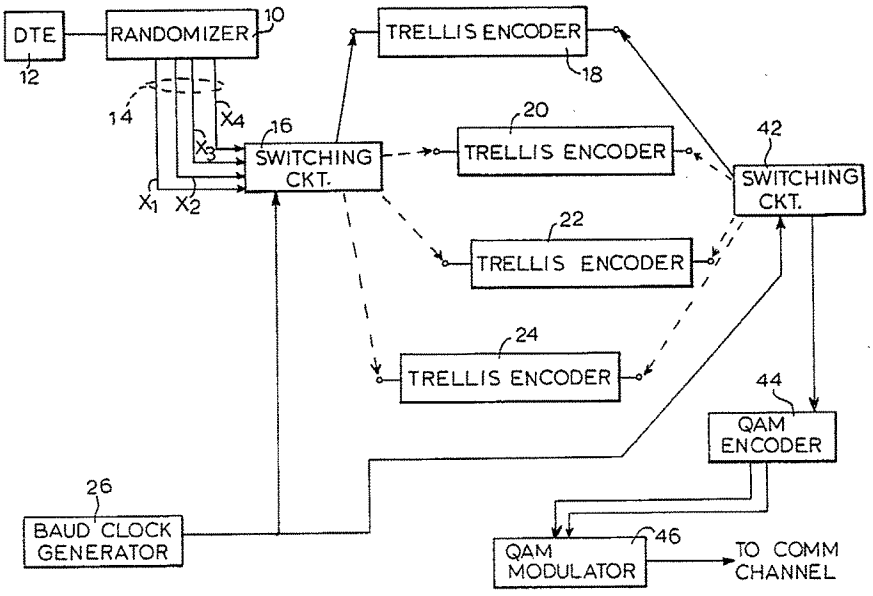
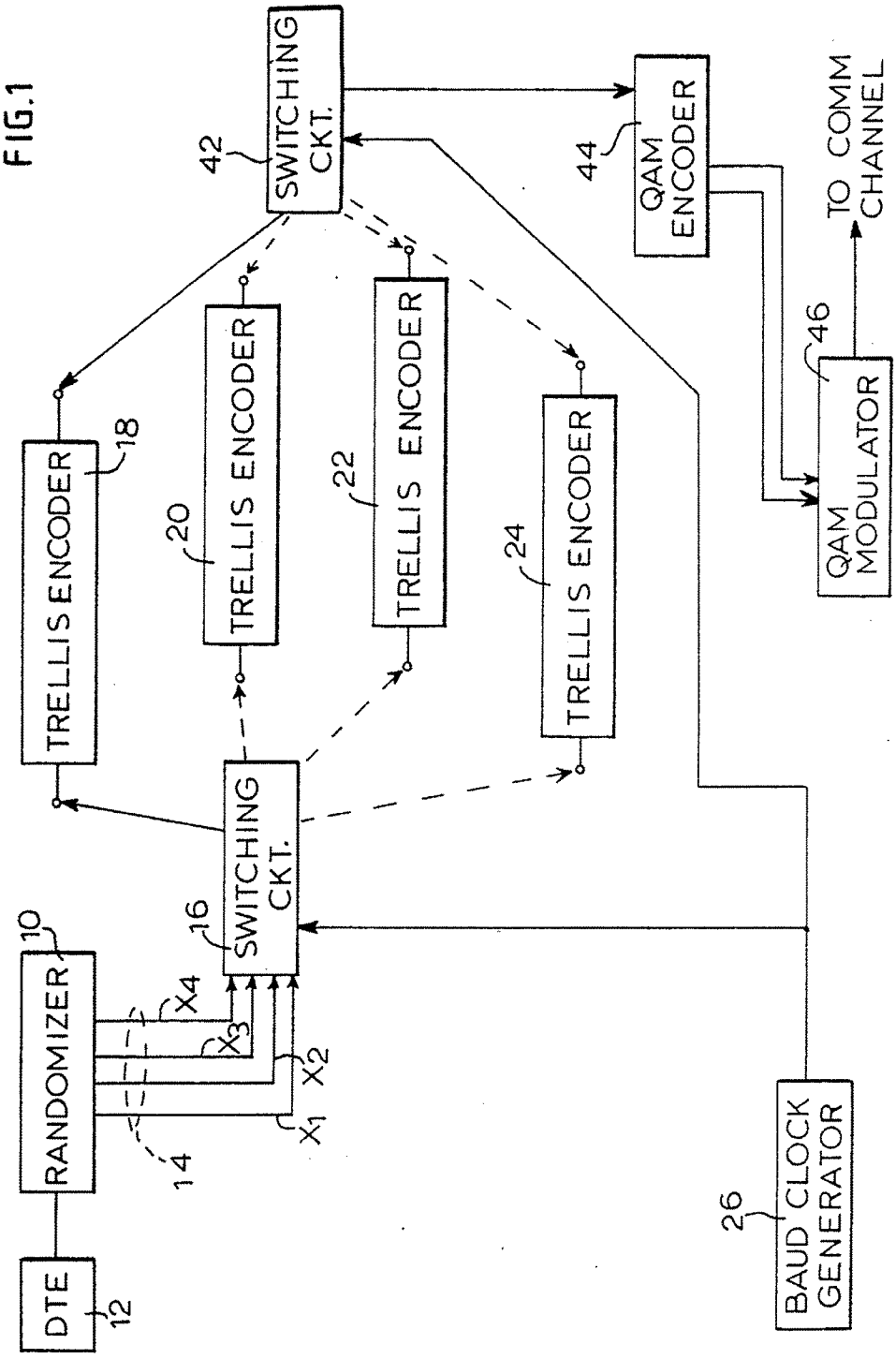


FIG.1


SWITCHING CKT.
42
QAM ENCODER
44
TO COMM CHANNEL
46
QAM MODULATOR
TRELLIS ENCODER
18
TRELLIS ENCODER
20
TRELLIS ENCODER
22
TRELLIS ENCODER
24
SWITCHING CKT.
16
RANDOMIZER
10
X4
X3
X2
X1
14
DTE
12
BAUD CLOCK GENERATOR
26

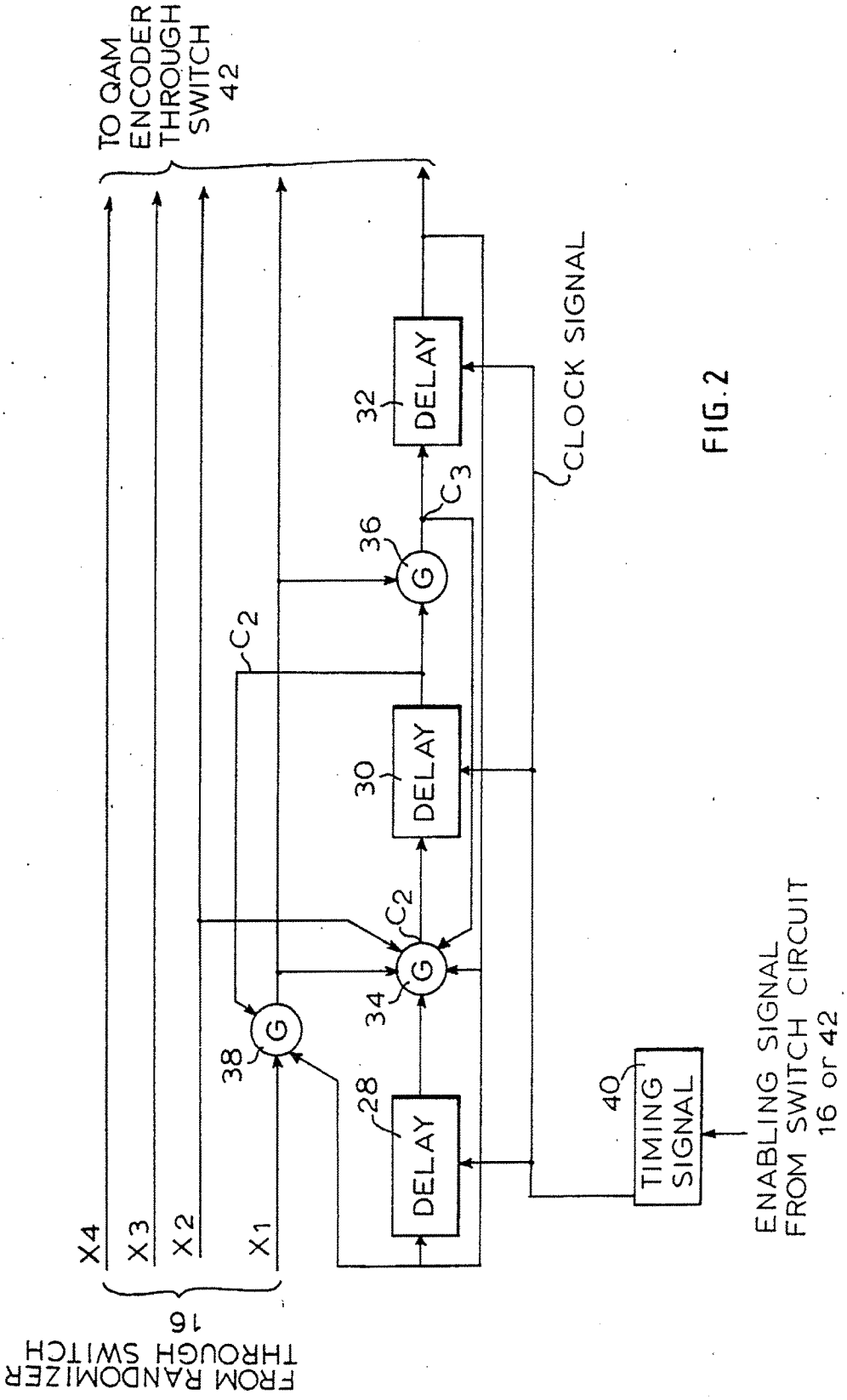
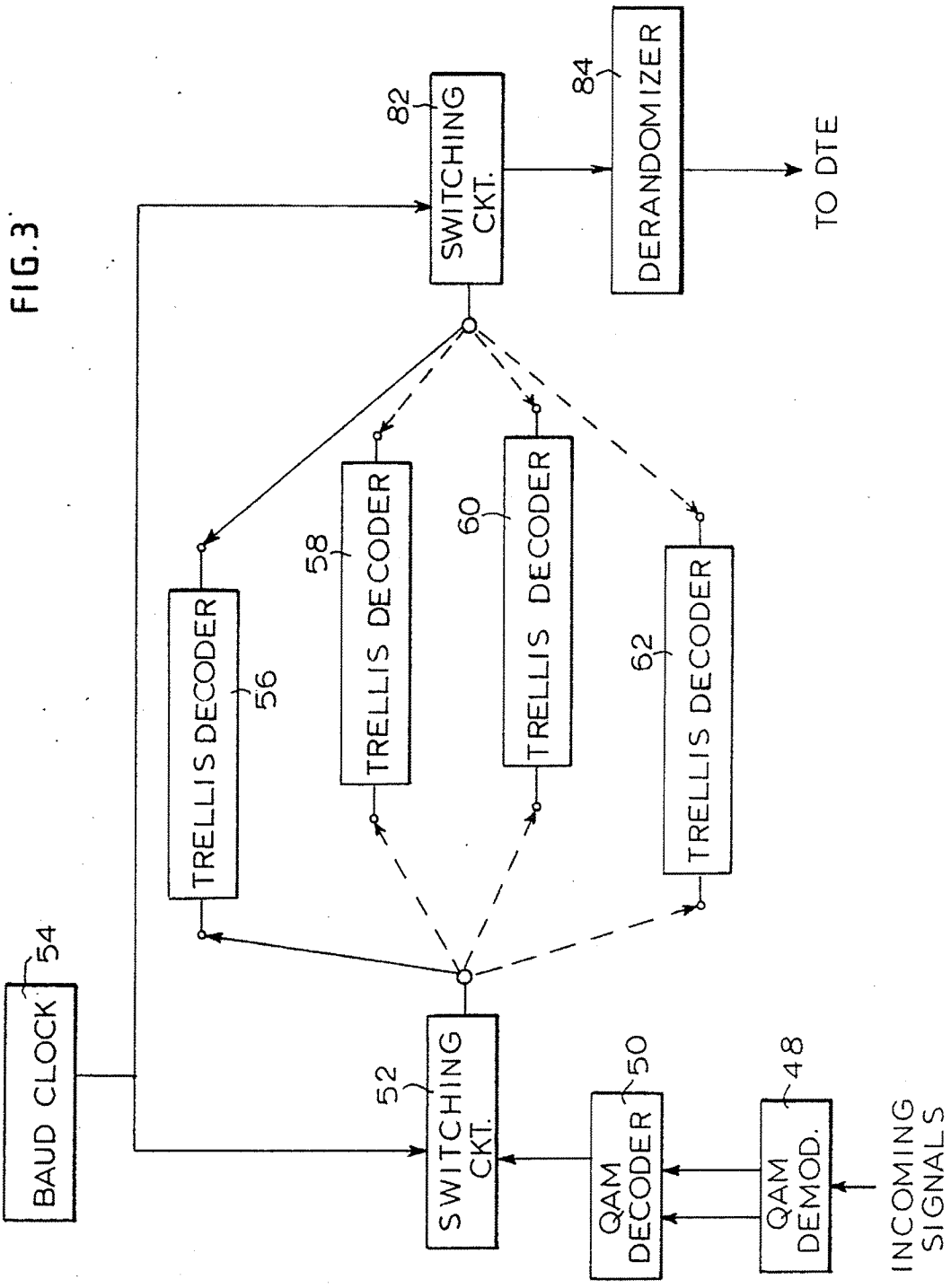

TO QAM ENCODER THROUGH SWITCH 42
CLOCK SIGNAL
DELAY
32
DELAY
30
DELAY
28
G
36
G
34
G
38
C3
C2
C2
X4
X3
X2
X1
16
FROM RANDOMIZER THROUGH SWITCH
TIMING SIGNAL
40
ENABLING SIGNAL FROM SWITCH CIRCUIT 16 or 42

FIG. 2

FIG. 3


BAUD CLOCK
54
SWITCHING CKT.
52
QAM DECODER
50
QAM DEMOD.
48
INCOMING SIGNALS
TRELLIS DECODER
56
TRELLIS DECODER
58
TRELLIS DECODER
60
TRELLIS DECODER
62
SWITCHING CKT.
82
DERANDOMIZER
84
TO DTE

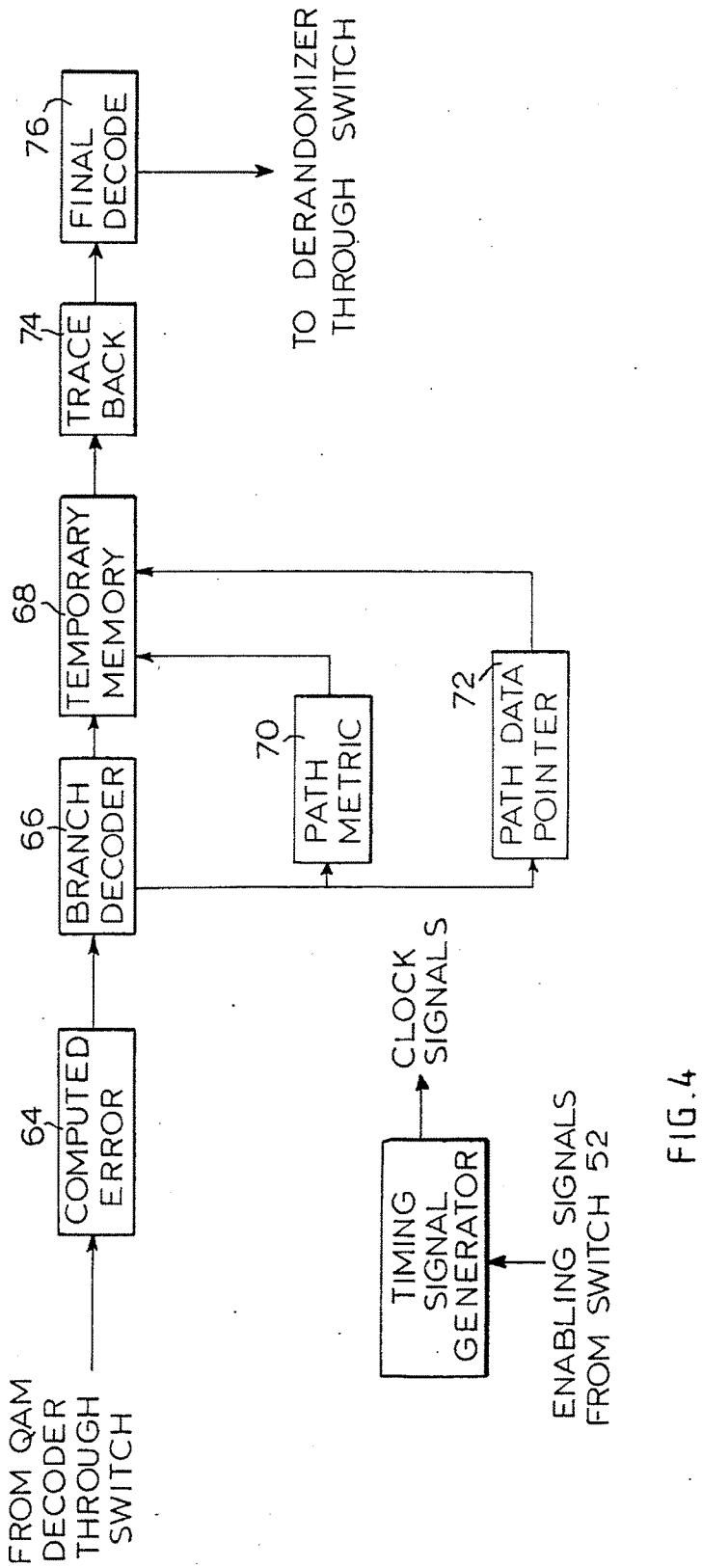

FROM QAM DECODER THROUGH SWITCH
64
COMPUTED ERROR
66
BRANCH DECODER
68
TEMPORARY MEMORY
70
PATH METRIC
72
PATH DATA POINTER
74
TRACE BACK
76
FINAL DECODE
TO DERANDOMIZER THROUGH SWITCH
TIMING SIGNAL GENERATOR
CLOCK SIGNALS
ENABLING SIGNALS FROM SWITCH 52

FIG. 4

DISTRIBUTED TRELLIS ENCODER

RELATED APPLICATIONS

The subject matter of this application is related to U.S. applications Ser. No. 707,085 entitled Self-Synchronizing Interleaver for Trellis Encoder used in Wireline Modems and Ser. No. 707,083 entitled Self-Synchronizing De-Interleaver for Viterbi Decoder Used in Wireline Modems, filed on even date herewith and incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of Invention

This invention pertains to an apparatus and method of encoding binary bits and more particularly to a method and apparatus for making use of a forward error correction scheme for a reduced number of errors at a given signal-to-noise ratio.

2. Description of the Prior Art

Communication networks using high speed data rates require high signal-to-noise ratios for proper data transmission. Numerous schemes and combinations thereof have been proposed to reduce the number of errors at these given signal-to-noise ratios. For example, in U.S. Pat. No. 4,077,021 to Csajka et al a forward error correcting scheme is described making use of the so-called Viterbi algorithm. In a further development described by the CCITT study group XVII, Contribution No. D180, in October, 1983, entitled TRELLIS-CODED MODULATION SCHEME WITH 8-STATE SYSTEMATIC ENCODER AND 90 SYMMETRY FOR USE IN DATA MODEMS TRANSMITTING 3–7 BITS PER MODULATION INTERVAL a two-dimensional trellis for a quadrature amplitude modulation scheme is disclosed having 90° symmetry which results in a 4db gain in the signal-to-noise ratio. Typically, in forward error coding, redundant bits are added systematically to the data bits so that normally only predetermined transitions from one sequential group of bits (corresponding to bauds) to another are allowed. There is an inherent correlation between these redundant bits over consecutive bauds. At the receiver each baud is tentatively decoded and then analyzed based on past history, and the decoded bits are corrected if necessary. However, it was found that certain types of relatively long error signals, such as for exmaple, low frequenty phase jitter, cause a constant phase error in the signal constellation for extended (consecutive baud) periods of time. This type of error prevents or inhibits the correction of the received bits using the schemes described above.

OBJECTIVES AND SUMMARY OF THE INVENTION

A principal objective of the present invention is to provide a device and method for data communication in which the effects of long bursts of error signals such as low frequency phase jitter are minimized.

A further objective is to provide a method of adapting a standard modem to perform the subject method and to provide a method that is self-synchronizing.

Other objectives and advantages of the invention shall become apparent from the following description of the invention.

In the present invention the correlation of the redundant bits of different baud signals is distributed in time prior to encoding at the transmitter. A distributed trellis encoding scheme is used to obtain the redundant bits. At the receiver the received bauds are decoded using a plurality of distributed decoders which extract samples from multiple bauds for trellis decoding. The result is similar to that achieved by interleaving but avoids synchronization problems associated with the conventional complex interleaving processes.

BRIEF DESCRIPTION OF THE FIGURES

FIG. **1** shows the elements of a data transmitter constructed in accordance with the invention;

FIG. **2** shows the elements of a distributed trellis encoder;

FIG. **3** shows the elements of a receiver for receiving data from the transmitter of FIG. **1**; and

FIG. **4** shows the elements of a distributed trellis decoder.

DETAILED DESCRIPTION OF THE INVENTION

As shown in FIG. **1**, a transmitter according to this invention comprises a randomizer **10** which receives serially a stream of data bits from DTE **12**. The randomizer scrambles the bits in a preselected pattern and generates randomized bits on parallel output lines **14** identified as X1, X2, X3 and X4.

These output lines are fed by an electronic switching circuit **16** to a plurality of identical trellis encoders **18**, **20**, **22** and **24**.

The electronic switching circuit **16** switches the signals from the randomizer **10** to one of the trellis encoders **18**, **20**, **22** and **24**, in accordance with a baud clock signal generated by baud clock generator **26**. In other words, for each baud period all the randomizer outputs X1, X2, X3 and X4 are fed to one of the encoders. Details of the trellis encoders **18**, **20**, **22** and **24** are shown in FIG. **2**.

Each encoder comprises three delay units **28**, **30** and **32** which are adapted to generate a delay of one baud period. The encoder further comprises three gates **34**, **36** and **38**. These gates may be for example XOR (exclusive -OR) gates.

The trellis encoder shown in FIG. **2** is well known in the art and need not be described any further. Preferably all the elements of the encoder are digital elements which are enabled by appropriate clocking signals from timing signal generator **40**. The timing signal generator is enabled only when it receives an appropriate signal from switching circuit **16**. Thus each encoder is active only when it is addressed by switching circuit **16**. At all other times, the trellis encoders are idle.

Outputs Y0, Y1, X2, X3 and X4 are fed from the respective trellis encoders by a second electronic switching circuit **42** to QAM (quadrature amplitude modulation) encoder **44**. Switching circuit **42** is also enabled by baud clock generator **26** so that it operates simultaneously with switching circuit **16**. QAM encoder **44** selects a point of a preselected signal constellation corresponding to the inputs from circuit **42** and generates an in-phase and a quadrature output signal corresponding to said point. These output signals are fed to a QAM modulator **46** which generates corresponding analog QAM signals having a baud period equal to the period of the signals generated by signal generator **26**. The signals from modulator **46** are transmitted over a common data communication channel to a receiver.

In effect the bits of several consecutive signals are spaced out over several bauds by the distributed trellis encoders.

At the receiver, illustrated in FIG. 3, the incoming analog signals are demodulated by a QAM demodulator 48 which generates an in-phase and a quadrature signal which are fed to a QAM decoder 50. The QAM decoder 50 selects a point on the signal constellation closest to the actual point corresponding to the signals received from QAM demodulator 48. The bits corresponding to said point are sent to a third electronic switching circuit 52 having a period equal to the baud period of the received signals. Circuit 52 accesses sequentially one of four distributed trellis decoders 56, 58, 60 and 62 in response to the switching signal from generator 54. Thus all the binary signals from QAM decoder 50 corresponding to each received QAM signal are sent to one of the trellis decoders. The four trellis decoders are standard decoders well known in the art. One such decoder is shown in FIG. 4.

In a typical trellis decoder, the signals from the QAM decoder (in the present case, via switching circuit 52) are fed into an error computer circuit 64 which generates an error signal based on previously received signals. This error signal is fed to a branch decoder 66. The branch decoder uses the trellis branch rules (predetermined in accordance with the Viterbi algorithm) to generate a set of possible points corresponding to the received point. These set of points are stored in temporary memory 68. The decoder then searches through the points of the set to calculate the point with the smallest errors in accordance with appropriate constants stored in the path metric memory 70 and path pointer memory 72. The smallest error is used by trace back memory 74 to track back the last 4–16 bauds (in accordance with a preselected well-known scheme) to generate the final received point. The final received point of the set of points in memory 68 is fed to final decoder 76 as the received point.

As with the encoder of FIG. 2, each decoder comprises digital elements which are enabled by a timing signal generator 78.

The timing signal generator is enabled by an appropriate signal from switching circuit 52 only when the respective decoder is addressed by the switching circuit. Generator 78 generates clocking signals for the various decoder elements. Thus each decoder 56, 68, 60 and 62 is active only when it is addressed by switching circuit 52, and otherwise it is idle.

The output of each decoder is accessed sequentially by a fourth electronic switching circuit 82 which is synchronized by the baud clock generator 54 so that it is in step with switching circuit 52. In other words, each trellis decoder is accessed simultaneously by switch circuits 52 and 82. The switching circuit 82 feeds the signals from the decoders to derandomizer 84 for reversing the effects of randomizer 10 and then to a user DTE.

It can be seen from the above description that switching circuits 16 and 52 acts as multiplexers while switch circuits 42 and 82 act as demultiplexers. The effect of this switching is to interleave the data bits at the transmitter across four bauds, and deinterleave these bits at the receiver. Obviously the trellis encoders are self-synchronized so that no synchronizing signals are needed between the transmitter and receiver

In the above description consecutive bits are interleaved across four bauds by using four distributed trellis encoders and decoders. Obviously if more encoders and decoders are used the number of bauds over which interleaving occurs increases.

It should be appreciated that the invention makes use of standard QAM encoders, modulators, decoders, demodulators and standard trellis encoders and decoders which are well known in the art. Furthermore, while baud clock generators 26 and 54 are described as separate elements, in practice they can be incorporated in the QAM modulator and demodulator respectively. All the circuits of FIGS. 1 and 3 may be implemented by using a digital microprocessor.

Obviously, numerous modifications to the subject application may be made without departing from the scope of the invention as defined in the appended claims.

What is claimed is:

1. A data transmission section for a modem coupled to a channel for sending data signals comprising:
   1. A plurality of trellis encoders, each trellis encoder having an input for receiving n plain text bits, each encoder being provided to interleave bits received by the encoder during a first baud period with bits received during more than two previous baud periods to generate n trellis encoded bits, k, being larger than one; in a single baud period, each trellis encoder having means for delaying at least some of said n plain text bits so that they may be outputted and combined with bits outputted from one or more other trellis encoders during single baud periods;
   2. encoder activating means for selectively activating only one of said trellis encoders for one baud period in a preselected sequence whereby bits received during a baud period i are interleaved with bits received during a baud period i-k;
   3. signal encoding means for converting encoded bits into signals suitable for transmission over said channel; and
   4. transmitter switching means for feeding n plain text bits per baud period to the activated trellis encoder and for sending the encoded bits from the activated trellis encoder to the signal encoding means.

2. A receiver section for a modem receiving data signals from a channel, said signals having been trellis encoded by interleaving bits corresponding to a baud period i with bits corresponding to a baud period i-k, k being larger than two, and having:
   1. a demodulator and a decoder connected to the output of said demodulator for converting analog data signals from said channel into multiple series of bits, each series of bits substantially corresponding to a point of said analog data signal's preselected signal constellation;
   2. k trellis decoders, each trellis decoder having an input from said decoder for receiving series of bits from said decoder and generating n bits of plain text bits corresponding to n bits received at least during two previous baud periods;
   3. decoder activating means for activating only one of said trellis decoders during one baud period in another predetermined sequence; and
   4. receiver switching means for feeding n encoded bits to the activated decoder and for collecting n plain text bits from the activated decoder.

3. A method of transmitting a plurality of input data bits over a channel by quadrature amplitude modulator comprising:

providing a plurality of trellis encoders, each encoder using an identical scheme to interleave bits received during a first baud period with bits received during more than two earlier baud periods preceding said first baud period to generate output bits;

activating each of said trellis encoders in a preselected order for a baud period;

feeding bits which occur during a single baud period to only one of said plurality of trellis encoders;

delaying at least some of said bits in said one trellis encoder during a single baud period;

combining bits which have been outputted from said one trellis encoder with bits which have been outputted from one or more different trellis encoders for transmission during a single baud period; and

quadrature amplitude modulating output bits of each activated trellis encoder.

4. A system for transmitting data signals over a data channel comprising:

a. a data transmission section coupled to said channel for sending data signals and having:

1. A plurality of trellis encoders, each trellis encoder having an input for receiving n plain text bits each encoder being provided to combine bits received by the encoder during more than two previous baud periods with bits received during a previous baud period to generate n trellis encoded bits in a single baud period, each trellis encoder having means for delaying at least some of said n plain text bits so that they can be outputted and combined with bits outputted from one or more other trellis encoders during single baud periods;

2. encoder activating means for selectively activating only one of said trellis encoders for one baud period in a preselected sequence;

3. signal encoding means for converting encoded bits into signals suitable for transmission over said channel; and

4. transmitter switching means for feeding n plain text bits per baud period to the activated trellis encoder and for sending the encoded bits from the activated trellis encoder to the signal encoding means; and

b. a receiver section for receiving data signals from said channel, and having:

1. a demodulator and a decoder connected to the output of said demodulator for converting analog data signals from said channel into multiple series of bits, each series of bits substantially corresponding to a point of said analog data signal's preselected signal constellation of;

2. a plurality of trellis decoders equal in number to the trellis encoders, each decoder generating n bits of plain text bits corresponding to n bits received by the encoder during a baud period and n bits received at least during a previous baud period;

3. decoder activating means for activating only one of said trellis decoders during one baud period in another predetermined sequence; and

4. receiver switching means for feeding n bits to the activated decoder and for collecting n plain text bits from the activated decoder.

5. The system of claim **4** wherein said transmitter switching means comprises a first transmitter switch for providing input bits to the activated trellis encoder, and a second transmitter switch for providing encoded bits from the activated trellis encoder to the signal encoding means.

6. The system of claim **5** wherein said signal encoding means comprises a quadrature amplitude modulator.

7. The system of claim **6** wherein said signal decoding means comprises a quadrature amplitude demodulator.

8. The system of claim **7** wherein there are k trellis encoders each trellis encoders including several delay elements for combining the bits received during said one baud periods with bits received during several preceding baud periods each preceding baud period being separated from the next baud period by $(k-1)$ D seconds where D is the duration of a period.

9. The system of claim **7** wherein said receiver switching means comprises a first receiver switch for feeding encoded bits to the activated decoders and a second receiver switch for collecting plain text bits from the activated decoders.

10. The system of claim **7** wherein each period has a time duration of D seconds and each encoder includes a delay element for delaying bits received during a baud period by D seconds.

11. The method of claim **3** further comprising providing a plurality of trellis decoders for sequentially decoding transmitted signals, each trellis decoder being activated sequentially for a baud period for deinterleaving said signals.

* * * * *